

Nano- and Micro-structured CdTe

Solar Cells



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Abstract

This thesis explores new geometries of CdTe solar cells to exploit nanowires (NWs) and microrods. Additionally it assesses the use of MgCl_2 as an alternative to CdCl_2 in CdTe processing for the first time in ‘substrate’ planar and NW devices and all-sputtered ‘superstrate’ planar and microrod devices.

Two methodologies were investigated for the fabrication of CdTe NWs by close-space sublimation growth: a) the selective-area method using ultra-thin sputtered holey films and antidot templates developed by nanosphere lithography and b) the vapour-liquid-solid using Au, Bi, Bi_2Te_3 , Sb, Sn and Pt catalysts. Growth of Au- and Bi-catalysts were the most effective yielding NWs with average diameters of 100-500 nm, lengths of 1-10 μm and densities of 10^6 - 10^7 cm^{-2} . However, Bi-growth was susceptible to irreproducibility and oxidation effects, making Au the option that was used in devices. Addition of NWs to 200 nm thick CdTe films reduced the optical transmittance and reflectance by two orders of magnitude. As an alternative to CdTe absorber NWs, ZnO microrods were available that had been electrodeposited on commercial transparent conducting oxides coated glass plates.

In order to evaluate the impact of both the CdTe NWs and ZnO microrods on devices, planar control devices were developed and these were modified by incorporating the NWs and microrods. The performance of a) planar and Au-catalysed NW CdTe solar cells in the ‘substrate’ configuration, i.e. Mo/CdTe/CdS/ITO and $\text{Mo/CdTe/CdTe(NWs)/CdS/ITO}$ and that of b) ZnO planar and ZnO microrod CdTe solar cells in the ‘superstrate’ configuration, i.e. $\text{TEC/ZnO/CdS/CdTe/Au}$ and $\text{TEC/ZnO/ZnO(microrods)/CdS/CdTe/Au}$ were evaluated and compared to record-efficiency devices. All devices were processed using MgCl_2 and demonstrated competitive efficiencies, these being up to $8.5 \pm 0.1\%$ and $2.1 \pm 0.1\%$ for the planar and CdTe NW ‘substrate’ devices and up to 13.28% and 6.18% for the ZnO planar and ZnO microrod devices respectively. It is postulated that the main performance limitations are a) the rectifying back contact and electrical shunting in both ‘substrate’ devices and b) excessive voiding in the microrod ‘superstrate’ devices.

The results of this work show that a) NWs exhibit low optical losses and b) MgCl_2 can be used instead of the highly-toxic CdCl_2 with efficiencies comparable to those of published elsewhere. Suggestions to further improve the performance of all PV device architectures in this work are given.

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Αφιερώνω τη διδακτορική μου διατριβή με όλη μου την αγάπη στην οικογένειά μου, Ελένη, Κώστα, Ελευθερία και Άρη.

Contents

1 Introduction.....	1
1.1 References	8
2 Solar cell device characteristics and CdTe thin film devices	9
2.1 Introduction	9
2.2 Solar Cell characteristics.....	10
2.2.1 Semiconductor junctions.....	10
2.2.2 The photovoltaic effect	15
2.2.3 J-V characteristics of solar cell devices	16
2.2.4 Shockley-Queisser limit.....	23
2.2.5 Losses in real solar cell devices	25
2.3 CdTe solar cell device technology	29
2.3.1 Material properties of CdTe.....	29
2.3.2 Device structure	30
2.3.3 Cl treatment.....	34
2.3.4 Progress review of the CdTe PV performance	34
2.4 References	35
3 Nanowire growth and nanowire-based solar cells	40
3.1 Introduction	40
3.2 Semiconductor nanowire growth techniques	41
3.2.1 Top-down approach	41
3.2.2 Bottom-up approach.....	41
3.2.3 Review on the growth of CdTe nanowires	46
3.3 Nanowire photovoltaic devices	48
3.3.1 Nanowire solar cell heterostructures.....	48
3.3.2 Advantages of nanowire over planar devices	50
3.3.3 Challenges in the development of nanowire devices	53
3.4 Review on nanowire solar cell devices	57
3.4.1 State of the art nanowire PVs.....	57
3.4.2 CdTe nanowire PVs	58
3.5 References	60
4 Experimental methods.....	72
4.1 Introduction.....	72
4.2 Thin film and nanowire growth techniques	72
4.2.1 Close-space sublimation	72
4.2.2 Magnetron sputtering	74
4.2.3 Thermal evaporation	76
4.2.4 Spin coating	77
4.3 Thin film and nanowire characterisation techniques	78
4.3.1 Contact stylus profilometry.....	79
4.3.2 Scanning electron microscopy and microanalysis	79
4.3.3 X-ray diffraction	82

4.3.4 Optical spectroscopy	86
4.3.5 Spectroscopic ellipsometry	87
4.3.6 Atomic force microscopy	88
4.3.7 Raman spectroscopy	89
4.4 Solar cell performance characterisation	90
4.4.1 J-V measurements	90
4.4.2 J-V-T measurements	91
4.4.3 C-V measurements	91
4.4.4 EQE measurements	92
4.5 References	94
5 Growth studies of CdTe nanowires using template assisted and vapour-liquid-solid growth methods	97
5.1 Introduction	97
5.2 Experimental	99
5.2.1 Experimental procedures and growth conditions	99
5.2.2 Sample sets	105
5.3 Investigation of the template assisted, catalyst-free growth of CdTe nanowires	106
5.3.1 Development of holey templates	106
5.3.2 Development of antidot templates	107
5.3.3 CdTe growth using holey and antidot templates	110
5.3.4 Discussion of the templated growth study of CdTe nanowires	111
5.4 Growth of CdTe nanowires using Au catalysts	114
5.4.1 Development of Au nanodot arrays	114
5.4.2 Morphology and elemental composition of CSS-grown Au-catalysed CdTe nanowires	117
5.4.3 Investigation of the CdTe nanowire growth orientation	120
5.4.4 Effect of Au film thickness, deposition time, pressure and temperature on the growth of CdTe nanowires	122
5.4.5 Discussion of the Au-catalysed VLS growth of CdTe nanowires	128
5.5 Growth of CdTe nanowires using Bi catalysts	139
5.5.1 Development of Bi nanodot arrays	139
5.5.2 Nanowire growth in N ₂ ambient	143
5.5.3 Nanowire growth in H ₂ ambient	144
5.5.4 Discussion of the Bi-catalysed growth of nanowires	148
5.6 Conclusions	156
5.7 References	160
6 Planar and core/shell nanowire CdTe/CdS solar cells grown on molybdenum substrates	166
6.1 Introduction	166
6.2 Experimental	167
6.2.1 Growth conditions	167
6.2.2 Sample sets	169
6.3 Optical properties of planar and nanowire CdTe layers	171

6.4 Optimisation of the MgCl_2 activation process of planar and NW ‘substrate’ CdTe/CdS on Mo foils	174
6.5 Electrical characterisation of the highest efficiency planar and nanowire CdTe/CdS devices.....	176
6.5.1 J-V.....	176
6.5.2 EQE.....	178
6.6 Discussion	180
6.6.1 Optimisation of the MgCl_2 process.....	180
6.6.2 Performance losses in the NW devices	181
6.6.3 Comparison of highest efficiency NW device to record efficiency CdTe NW-based devices	184
6.6.4 Comparison of highest efficiency planar device to record efficiency ‘substrate’ CdTe/CdS devices.....	186
6.7 Conclusions.....	188
6.8 References	191
7 All-sputtered CdTe/CdS solar cells grown on planar and microrod ZnO coated glass substrates	193
7.1 Introduction	193
7.2 Experimental	195
7.2.1 Growth conditions of sputtered CdTe solar cells in the planar and microrod geometries	195
7.2.2 Sample sets.....	200
7.2.3 Characterisation techniques	203
7.3 Planar CdTe/CdS solar cell devices	204
7.3.1 The effect of the CdS window layer thickness	204
7.3.2 The effect of the CdTe absorber layer thickness	206
7.3.3 Post- MgCl_2 back surface characterisation and etching studies.....	208
7.3.4 Back contact buffer layers	216
7.3.5 Electrical characterisation of highest efficiency planar device.....	221
7.3.6 Discussion of planar device properties	228
7.4 CdTe/CdS solar cell devices developed on ZnO microrod coated substrates..	242
7.4.1 SEM/EDX investigation of the CdTe/CdS microrod devices development	242
7.4.2 Electrical characterisation of highest efficiency microrod device	245
7.4.3 Comparison of planar and microrod CdTe/CdS devices by means of Raman and optical spectroscopy	253
7.4.4 Discussion of microrod materials and devices and comparison with planar devices.....	259
7.5 Conclusions.....	264
7.6 References	268
8 Conclusions and future work.....	274
8.1 Research overview, key findings and implications.....	274
8.2 Future work	276
8.2.1 Selective-area growth of CdTe nanowires	276
8.2.2 Metal-catalysed VLS growth of CdTe nanowires	277

8.2.3 ‘Substrate’-geometry nanowire CdTe/CdS solar cells.....	277
8.2.4 ‘Substrate’-geometry nanowire and planar CdTe/CdS solar cells	278
8.2.5 ‘Superstrate’-geometry microrod CdTe/CdS solar cells	279
8.2.6 ‘Superstrate’-geometry microrod and planar CdTe/CdS solar cells	279
Appendix A: Growth of Bi-catalysed CdO nanowires	281
A.1. Introduction.....	281
A.2. Experimental	281
A.3. Results.....	282
A.4. Discussion	284
A.5. Conclusions.....	287
A.6. References.....	287
Appendix B: Assessment of alternative catalysts for the VLS growth of CdTe nanowires	288
B.1. Introduction.....	288
B.2. Experimental	288
B.3. Results.....	289
B.4. Conclusions.....	290

1 Introduction

The global primary energy supply is estimated to 155000 TWh with more than 80% of it coming from burning fossil fuels¹. The current forecasts² predict an increase in world energy consumption of 28% between 2015 and 2040, a trajectory which threatens to destabilise Earth's climate and mankind's prosperity and growth: Fossil fuels are limited, unevenly distributed and dirty. While depletion of reserves may become more alarming in the next 50-100 years, climate change and global warming require immediate action. An important first step to this end is the Kyoto protocol³, signed in 1997 by 192 countries (including EU) legally binding them to reduce greenhouse gas emissions. In 2020, it will be replaced by the Paris Agreement⁴, which was negotiated at the COP-21 Summit in 2015 with the main aim to maintain the global temperature rise below 2°C compared with pre-industrial levels. This highlights the necessity of a rapid transition from fossil fuels to more clean and sustainable technologies for energy generation. However, although the use of renewables is continuously rising, currently they account for only ~ 20% of the global energy generation⁵.

Photovoltaics (PV) have the potential to make a major contribution to this transition: the total annual solar irradiation reaching Earth is more than 7500 times the world's

total annual energy consumption and an order of magnitude greater than all non-renewable energy resources. In addition to this, it is a modular and scalable technology that can be deployed according to the needs: on- and off-grid systems, solar parks, domestic roof solar cells, building integrated PVs or solar-powered portable applications. Without the need of moving parts, solar panels require minimal maintenance and have performance warranties that guarantee a minimum of 90% of the initial solar cell efficiency even after 25 years⁶. In 2016, solar cells accounted for 47% of the total renewable energy installations⁵ with the electricity costs from PVs continuously falling.

Currently, the PV market is dominated by Si solar cells, which in 2016 had a share of 94% of global PV production⁷. The key factors of silicon's success in PV manufacturing are the established silicon-based microelectronics industry and silicon's abundance in Earth's crust in the form of quartzite. Nevertheless, due to its inherent technology limitations, such as an indirect bandgap, low absorption coefficient and expensive purification stages that are required for high-grade material, alternative technologies have emerged over the last twenty years. In particular, thin-film PV technology namely CdTe and Cu(In,Ga)Se₂ (CIGS) solar cells have achieved significant performance and stability improvements. Specifically, First Solar, the dominant player in the CdTe PV industry, has reported laboratory (~ 22.1%) and module (~ 18.6%) efficiencies, these being comparable to those of Si devices⁸.

One of the key advantages of CdTe over Si is the direct bandgap of ~ 1.45 eV, which enables optimal absorption of the solar radiation. Thus, high-efficiency CdTe solar cells are much thinner than Si solar cells adding significantly to cost reductions. In addition to this, CdTe solar cells have broader spectral response, lower temperature coefficient

and a linear response to shading, which enables them to produce up to 10% more power than comparable Si modules. Nevertheless, CdTe's PV efficiency is limited by their relatively low open-circuit voltage this being $\sim 60\%$ of the bandgap value⁹. This is mainly due to the low carrier density and excessive carrier recombination phenomena related to the polycrystalline nature of CdTe solar cell devices. These limitations are explored further in Chapter 2.

In recent years, nanowire (NW) solar cell architectures have been investigated for improving the performance and reducing the manufacturing costs of solar cell devices – this is reviewed in Chapter 3. Theoretically, nanowire devices can have superior performance to planar devices benefiting from enhanced light absorption, lower reflection losses, strain relaxation effects and improved carrier generation/collection properties. Furthermore, high-quality single-crystal nanowires can be grown without the need of expensive substrates or processes that are required in the manufacturing of single-crystal planar films. Thus, similar or even higher power conversion efficiencies compared to planar devices can be potentially achieved with potentially reduced manufacturing costs.

It is an important feature of these nanowire-based solar cell designs that few actually rely on quantum confinement effects for their operation. Indeed most 'nanowires' reported for use in PV devices have diameters of >200 nm, this being above the length scale for quantum confinement. Instead, practical devices can potentially realise performance advantages from a) light trapping in the wall of nanowires, b) the reduced lengths scales for carrier transport (reduction of recombination) and c) the avoidance of crystal defects in single crystal nanowires. Nevertheless, the term 'nanowires' is in

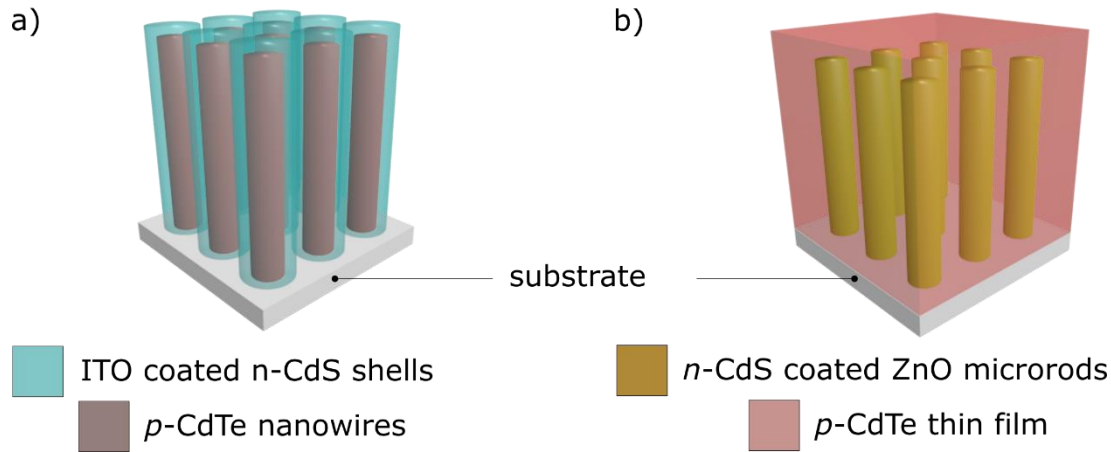


Fig. 1.1 Schematic illustrations of the radial and embedded architectures investigated in this work: a) radial core-shell p -CdTe/ n -CdS/ITO nanowires and b) n -CdS coated ZnO microrods embedded in a p -CdTe thin film.

common use and will therefore be used throughout this thesis. Where larger structures are referred to as ‘microrods’ as appropriate.

In this work, the implementation of two different nanowire (NW) solar cell architectures (Chapters 6 and 7) was investigated as shown in Fig. 1: a) p -CdTe nanowires grown on a CdTe-coated Mo foil were coated with n -CdS, while a transparent contacting oxide (TCO), in this case indium tin oxide (ITO) was used as a front contact (Chapter 6). b) n -CdS-coated ZnO microrods grown on a TCO-coated glass were embedded in a p -CdTe thin film (Chapter 7). In both cases, a radial PV junction is formed at the p -CdTe/ n -CdS interface and light enters the device from the side of the TCO. In order to optimize and evaluate their performance, equivalent planar devices, i.e. ‘substrate’- and ‘superstrate’-geometry p -CdTe/ n -CdS thin-film solar cells were also developed.

An overview of this thesis and a simplified flowchart (Fig. 1.2) of the nanowire growth and solar cell device fabrication experiments are given below.

- Chapter 2 describes the key aspects of semiconductor junctions and photovoltaics and outlines the fundamental performance limiting mechanisms. CdTe

solar cell technology is reviewed with a focus on the material properties and the two different device configurations: ‘substrate’ and ‘superstrate’, i.e. substrate/back contact/absorber layer/window layer/front contact and substrate/front contact/window layer/absorber/back contact. In both cases, light enters the device from the front contact.

- Chapter 3 outlines the most commonly-used nanowire growth methods and reviews the growth of CdTe nanowires with an emphasis on the selective area and vapour-liquid-solid (VLS) growth methods. The main NW solar cell device architectures, their potential advantages over planar devices and the main performance limiting factors are discussed. Finally, a review on the record-efficiency NW solar cell devices with a focus on CdTe-related NW-based devices is given.

- Chapter 4 describes the growth and characterisation experimental methods used in this thesis. It is divided in three main sections: a) thin film and nanowire growth, b) morphological, structural, optical and elemental characterisation of thin films and nanowire arrays and c) solar cell performance measurements.

- Chapter 5 investigates the growth of CdTe nanowires using two different methods: a) template-assisted catalyst-free nanowire growth and b) metal-catalysed VLS nanowire growth. While the template-assisted growth approach was less successful, the growth of Au- and Bi-catalysed CdTe NWs using the VLS growth method is reported. The spontaneous growth of Bi-catalysed CdO nanowires was also observed and is included in Appendix A. A broad range of alternative catalysts was also evaluated but were less effective (Appendix B).

- Chapter 6 describes the development of planar and NW-based CdTe solar cell devices in the radial core-shell geometry and compares their PV performance. First, the superior optical properties of the Au-catalysed CdTe NWs are demonstrated using UV-

VIS spectroscopy. Next, the application and optimisation of the novel MgCl_2 activation treatment for these devices is reported. PV performance measurements demonstrated peak efficiencies of $\sim 8\%$ for the planar devices and $\sim 2\%$ for the NW devices.

- Chapter 7 reports the development and characterisation of all-sputtered CdTe solar cells grown on planar and microrod ZnO coated substrates and assesses their PV performance. First, the device optimisation and in-depth characterisation of the CdTe planar devices, used as a guide for the development of the microrod devices is presented. The best-performing planar devices demonstrated efficiencies of up to $\sim 13\%$. Next, the chapter centres on the development and characterisation of the microrod devices. Evaluation of their performance showed peak efficiencies of $\sim 6\%$. To explain the performance discrepancy between planar and microrod devices, a comprehensive study of their morphological and optoelectronic properties was carried out.

- Chapter 8 gives an overview of the main achievements and research implications of this thesis. Finally, suggestions for future work indicated by the research are given.

Flowchart of nanowire growth and solar cell device development experiments

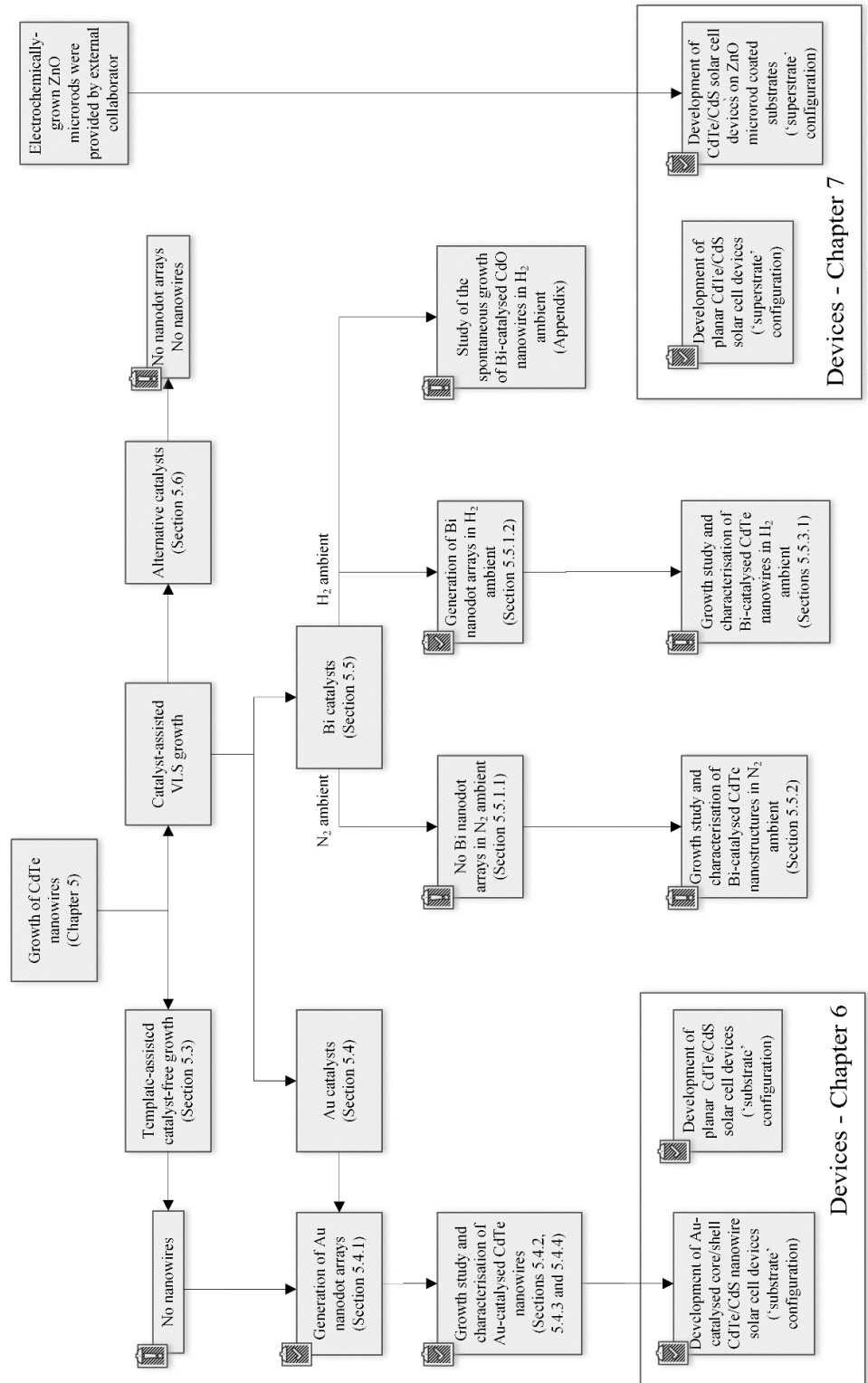


Fig 1.2 Flowchart of the nanowire growth and solar cell device fabrication experiments

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- ⁹ J. Sites, A. Munshi, J. Kephart, D. Swanson, and W.S. Sampath, in *2016 IEEE 43rd Photovolt. Spec. Conf.* (IEEE, 2016), pp. 3632–3635.

2 Solar cell device characteristics and CdTe thin film devices

2.1 Introduction

Solar cells or photovoltaics (PV) convert solar radiation directly into electricity. A solar cell device is essentially a large-area semiconductor p - n junction, which generates electric current via the photovoltaic effect. The main characteristics of single-junction solar cells are described in Section 2.2.3, while the fundamental performance limiting mechanisms are outlined in sections 2.2.4 and 2.2.5. In Section 2.3, the CdTe solar cell technology is reviewed with a focus on the material properties and the two different device configurations, i.e. ‘substrate’ and ‘superstrate’, and a description of the various component layers. Finally, one of the most critical steps in the development of high-performance CdTe solar cell devices, the CI treatment, is discussed.

The basic principles of semiconductor conductivity are well described in texts and will not be reviewed here. For reference the reader is directed towards the textbooks by Sze¹ and McCluskey² for descriptions of n - and p -conductivity, extrinsic (impurity) doping and intrinsic semiconductor behaviour.

2.2 Solar Cell characteristics

2.2.1 Semiconductor junctions

In this section, the three distinct semiconductor junction types, i.e. homo- and hetero-junctions and the semiconductor-metal Schottky junction are described together with an electrostatic analysis of the p - n junction.

2.2.1.1 The homo-junction

Fig 2.1 shows the formation of a homo-junction by joining n -type and a p -type layers made of the same semiconductor. Due to the electron and hole concentration gradients, electrons diffuse from the n -type layer to the p -type and holes from the p - to the n -type layer. This creates a space charge region or depletion region, which comprises fixed positively and negatively charged ions in the p - and n -type material respectively. The resulting electric field produces a drift current which opposes the initial diffusion current and, in equilibrium the two currents are equal, and a built-in potential V_{bi} is

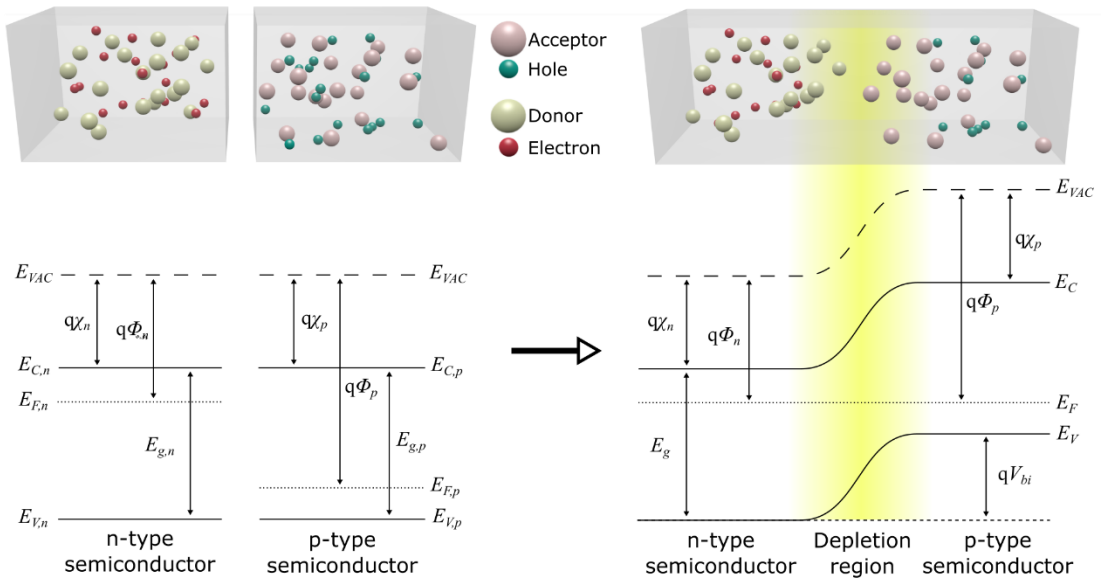


Fig. 2.1 Electronic band diagrams before and after the formation of a semiconductor homo-junction. Φ_n , Φ_p is the work function, χ_n , χ_p is the electron affinity, $E_{F,n}$, $E_{F,p}$ is the Fermi level, $E_{C,n}$, $E_{C,p}$ is the conduction band level, $E_{V,n}$, $E_{V,p}$ is the valence band level, $E_{g,n}$, $E_{g,p}$ is the band gap energy of the n - and p -type layers and V_{bi} the ‘built-in’ potential.

formed at the junction. The latter is determined from the difference in the work functions of the n - (Φ_n) and p -type (Φ_p) semiconductors.

The movement of the carriers and the formation of a charge imbalance at the interface affect the relative position of the various energy levels causing band bending. Its magnitude depends on the relative Fermi levels of the p - (Φ_p) and n -type (Φ_n) materials. Thus, in order to maintain a constant equilibrium Fermi level (E_F) across both the p - and n -layers, the band bends upwards in the p -type semiconductor and downwards in the n -type. The reader is referred to the texts by Sze¹ for a more detailed description of the semiconductor homo-junction.

2.2.1.2 The hetero-junction

Semiconductor hetero-junctions comprise p - and n -layers made of different semiconductor materials with different bandgap energies. Because of the variations in bandgap energy and valence and conduction band levels, spikes, notches and other discontinuities can occur upon band bending when the transition from the one semiconductor to the other takes places in an abrupt hetero-junction. Fig 2.2 (left) shows the band structure of such an abrupt hetero-junction, depicting the sudden energy change at the interface causing offsets in the conduction (ΔE_C) and valence (ΔE_V) bands. In reality, however, chemical interdiffusion is likely to occur between the two layers resulting in the formation of an intermixed layer. In practice such compositional grading may result in the smoothing of the abrupt interfacial features as shown in Fig 2.2 (right). The Cl activation of CdTe/CdS hetero-junction solar cells is a crucial step in achieving high PV efficiencies and, essentially, one of its effects is the conversion of the initially abrupt junction to a graded one³. Because of the large lattice mismatch (over 10%) between the CdTe and CdS layers, a high density of dislocations potentially occurs at the interface if the junction is abrupt. However, during the Cl activation step,

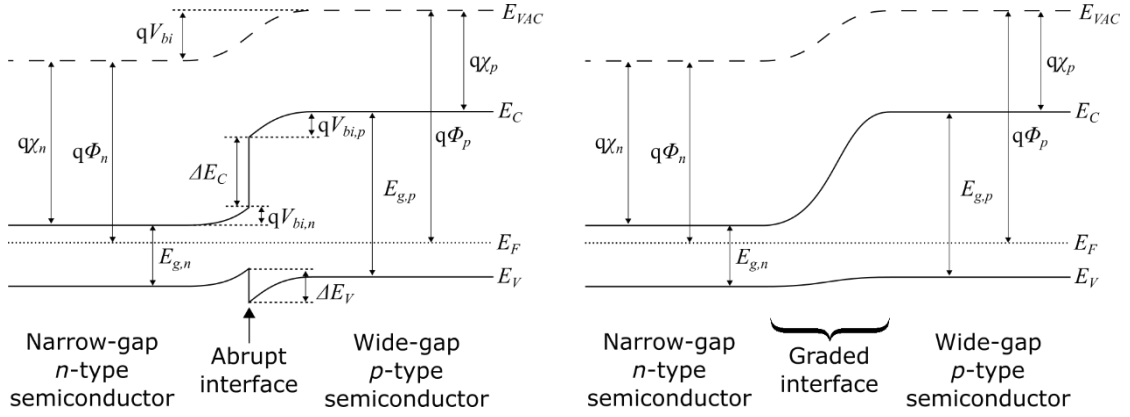


Fig. 2.2 Electronic band diagrams of an abrupt (left) and a graded (right) heterojunction. Φ_n , Φ_p is the work function, χ_n , χ_p is the electron affinity, $E_{g,n}$, $E_{g,p}$ is the band gap energy of the n - and p -type layers and E_F is the Fermi level, E_C is the conduction band level, E_V is the valence band level.

interdiffusion of S and Te between the two layers leads to the formation of a $\text{Cd}_x\text{S}_{1-x}\text{Te}$ intermixing layer, which, in turn, results in the formation of a graded junction. This acts to increase the overall junction quality and leads to enhanced PV performance.

2.2.1.3 The Schottky junction

Metal – semiconductor contacts can behave either as Ohmic contacts or as Schottky junctions, also called Schottky barriers. This depends on the electronic structures of the metal and the semiconductor. In particular, a Schottky junction to a p -type semiconductor is formed when the work function of the metal, Φ_m , is less than that of the semiconductor. Similarly to the formation of a semiconductor homo- or heterojunction, upon bringing the two layers together, holes diffuse from the semiconductor to the metal leaving negatively charged fixed ions behind. In Fig 2.3, the band diagrams of a metal, a p -semiconductor and that of the Schottky diode at thermal equilibrium are shown. Ideally the hole barrier height can be calculated from the energy difference between the valence band of the p -type semiconductor and the Fermi level of the metal as follows: $q\Phi = E_g + q\chi_p - q\Phi_m$. The formation of a Schottky barrier is typical in CdTe solar cell technology due to the work function of p -CdTe being ~ 5.9 eV, which

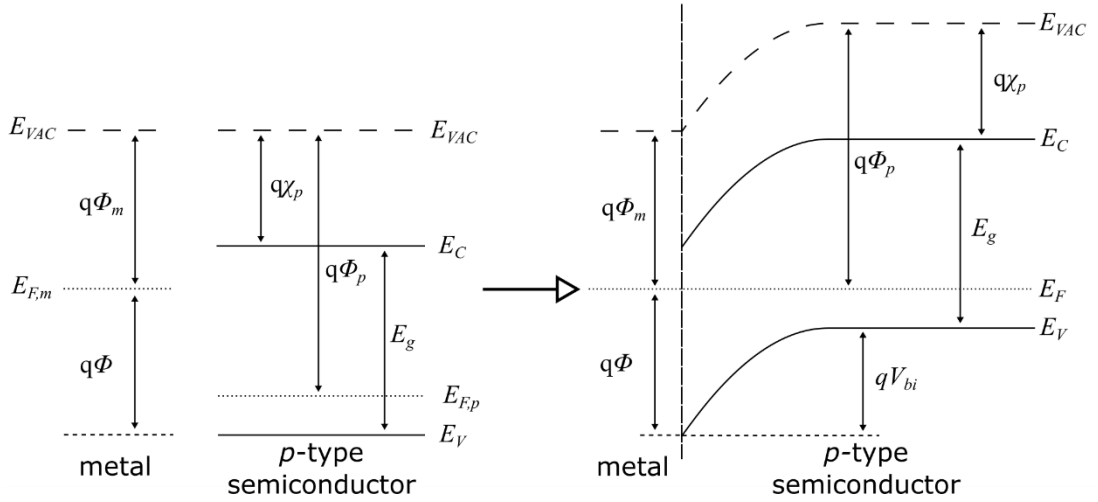


Fig. 2.3 Electronic band diagrams before (left) and after (right) the formation of a p -semiconductor-metal Schottky junction. $E_{F,n}$, $E_{F,p}$ is the Fermi level and Φ_n , Φ_p is the work function of the metal and the semiconductor layers, χ_p is the electron affinity, E_C is the conduction band level, E_V is the valence band level, E_g is the band gap energy of the semiconductor, V_{bi} the ‘built-in’ junction potential and Φ is the hole barrier height.

much higher to that of most metals¹. This is often found to have detrimental effects on the PV performance of CdTe solar cell devices⁴ and various solutions have been proposed, such as doping with Cu and incorporation of buffer layers⁵.

2.2.1.4 Electrostatics of a p - n junction

In a p - n junction the total built in potential is equal to $V_{bi} = V_{bi,n} + V_{bi,p} = \Phi_p - \Phi_n$ considering a constant doping profile in the p - and n -regions, a sharp doping transition at the p - n interface and no free charge carriers in the depletion region. An alternative expression¹ can be derived from the difference between the p - and n -type Fermi levels, since in equilibrium a constant Fermi level is expected throughout the junction:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right), \quad \text{Eq. 2.1}$$

¹ Commonly used metals with high work functions: Mo 4.6 eV, Au 5.15 eV, Pt 5.65 eV

where k is the Boltzmann's constant, T is the temperature and n_i the intrinsic carrier concentration.

By solving Poisson's equation, the depletion width can be calculated as follows:

$$W = w_n + w_p = \left[\frac{2\varepsilon_0 V_{bi} (\varepsilon_n N_D + \varepsilon_p N_A)}{q \varepsilon_n N_A N_D} \right]^{1/2}, \quad \text{Eq. 2.2}$$

where ε_0 is the free space permittivity and ε_n the relative permittivity of the n -type and ε_p that of the p -type semiconductor. However, it is often the case that the carrier concentration in the one part of the junction is much higher than in the other. In CdTe/CdS solar cells, the doping concentration in the CdS layer ($\sim 10^{17} \text{ cm}^{-3}$) is at least two orders of magnitude higher than in the CdTe layer ($\sim 10^{14-15} \text{ cm}^{-3}$). In this case, a one-sided junction is assumed which solely extends inside the CdTe layer and the can be approximated as:

$$W = \left[\frac{2\varepsilon_p \varepsilon_0 V_{bi}}{q N_A} \right]^{1/2} \quad \text{Eq. 2.3}$$

If an external voltage, V , is applied due to the relatively high resistivity of the depletion region, it acts as if it is applied directly across the junction. In this case, the depletion width can be calculated as follows:

$$W = \left[\frac{2\varepsilon_p \varepsilon_0 (V_{bi} - V)}{q N_A} \right]^{1/2} \quad \text{Eq. 2.4}$$

In a forward biased junction, more carriers are injected in the space charge region, which acts to lower its width. On the contrary, under reverse bias the majority carriers are pushed away leaving behind a higher number of charged ions, which increases the depletion region width.

The junction's capacitance is equal to

$$C = \frac{\epsilon_p \epsilon_0 A}{W}, \quad \text{Eq. 2.5}$$

where A is the junction's area. Using the previous expression for the depletion region width, one can determine the V_{bi} and N_A values by experimentally measuring the capacitance as a function of applied bias (C - V measurement). This is achieved by fitting the slope of the linear part of the $1/C^2 - V$ plot and using the derived expression:

$$\frac{d\left(\frac{1}{C^2}\right)}{dV} = \frac{2}{\epsilon_p \epsilon_0 A q N_A} \quad \text{Eq. 2.6}$$

For a more detailed description of the junction electrostatics and the derivation of the various formulae, the reader is referred to Refs.^{1,2}.

2.2.2 The photovoltaic effect

Photo-generated power, i.e. voltage and current, in solar cells is achieved via a process known as the photovoltaic effect. The first demonstration of the photovoltaic effect, the photogalvanic effect, dates 1839 by Becquerel⁶ using electrochemical cells and, later in 1876, Adams and Day⁷ demonstrated the photovoltaic effect in an all solid-state Se, Pt system. Since then a tremendous amount of research has been put in understanding the phenomenon and exploiting it for converting light into electrical energy. Indicatively, the first 'thin-film' device with an efficiency of 1% was developed in 1883⁸ and the first Si solar cell with an efficiency of 6% in 1954⁹. Today, the world record solar cell¹⁰ is a four-junction device able to convert 46% of the incoming radiation into electricity.

In a single-junction semiconductor solar cell, the photovoltaic effect occurs by the absorption of incident photons and the generation of free electrons in the conduction

band and holes in the valence band. However, in order for the generated carriers to be collected, the electron-hole pair needs to diffuse to the depletion region before the excited electron loses its excess energy and recombines with the hole. Upon successful diffusion to the depletion region, the charge carriers are separated by its electric field, i.e. the electron drifts to the n -part and the hole to the p -part. If the device is connected to an external load, the excess photo-generated electrons will flow from through the external circuit producing electrical power.

Light absorption in semiconductors arises from the electronic band structure. In direct bandgap semiconductors, such as CdTe, the maximum of the valence band (E_V^{max}) has the same wavevector, k , as the conduction band minimum (E_C^{min})¹. This enables the photoexcitation of a bound electron to a free state of the conduction band without a change in momentum (same wavevector) for photon energies $h\nu > E_g$. Photoexcited electrons at higher energy states of the conduction band will quickly relax close to the conduction band edge and the excess kinetic energy will be lost by thermalisation. If $h\nu < E_g$, the photon is not absorbed. On the contrary, in indirect semiconductors, such as Si, E_V^{max} and E_C^{min} have different k -values. Thus, due to the conservation of momentum, photoexcitation of electrons requires the additional absorption or emission of a phonon. The necessity of this additional process reduces the probability of photoexcitation and results in smaller absorption coefficients compared to those of direct semiconductors.

2.2.3 J-V characteristics of solar cell devices

In this section, an equivalent circuit of the ideal solar cell device is presented along with the main parameters that are used in the characterisation of the PV performance of solar cell devices.

2.2.3.1 Equivalent circuit models of ideal and real solar cell devices

An ideal solar cell device can be modelled using the *single diode model* which is derived from the solar cell physical principles². Under dark conditions, it is essentially consisted of a diode (*p-n* junction) and its current – voltage response is described by the Shockley equation^{11,12} as follows:

$$J = J_0(e^{qV_d/nkT} - 1), \quad \text{Eq. 2.7}$$

where J_0 is the reverse saturation current, V_d is the voltage across the diode and n is the *diode ideality factor*. The ideality factor is a measure of the junction quality and it is related to the current transport mechanisms across the junction and the bulk of a device. The reader is referred to Section 2.2.3.2 for further information on the carrier transport mechanisms of real devices and their effect on the ideality factor. Fig 2.4a shows the equivalent circuit of an ideal solar cell device under light, consisted of a diode and a current source connected in parallel (photovoltaic effect). Thus, the J - V response in this case is:

$$J = J_0(e^{qV_d/nkT} - 1) - J_L, \quad \text{Eq. 2.8}$$

where J_L is the photocurrent. In reality, however, circuit resistive losses, the series (R_S) and shunt (R_{SH}) resistance, should be taken in consideration and the resulting equivalent circuit is shown in Fig 2.4b. Therefore, the J - V response of a real solar cell device can be expressed as:

$$J = J_0(e^{q(V-AJR_S)/nkT} - 1) + \frac{V - AJR_S}{R_{SH}} - J_L, \quad \text{Eq. 2.9}$$

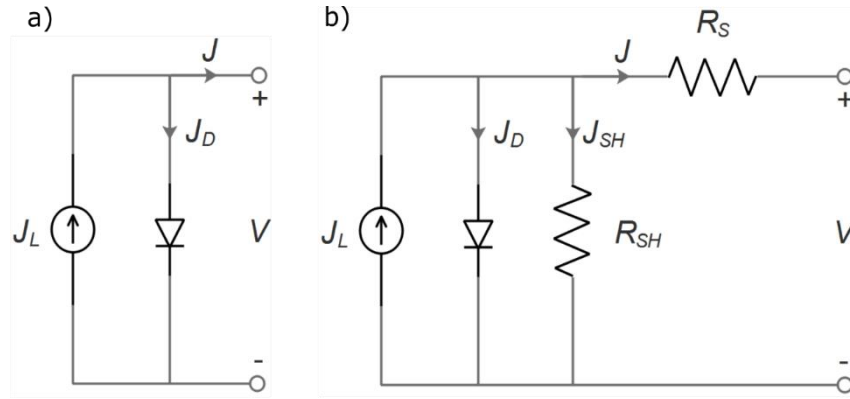


Fig. 2.4 The equivalent circuit of an ideal solar cell (a) and a real (non-ideal) solar cell (b) device.

by using $J_{SH} = \frac{V - AJR_S}{R_{SH}}$, where A is the area of the solar cell. The impact of R_S and R_{SH} on the J - V response of solar cell devices is analysed in detail in Section 2.2.5.3.

2.2.3.2 Carrier transport limiting effects

In a p - n junction, the charge carriers can flow through the junction and the bulk with several transport processes. In this section, the main carrier transport mechanisms that are typical in CdTe solar cells^{13,14} are described in order to understand and evaluate the J - V - T measurements that are presented in Chapter 7. The reader is referred to the PhD thesis of Al Turkestani¹⁵ for a comprehensive review of additional transport mechanisms that can take place in semiconductor p - n junctions.

Recombination and the ideality factor: In an ideal diode localised traps in the depletion region can act as recombination centres leading to further diffusion of minority carriers across the junction. According to the Shockley-Read-Hall theory, the recombination rate in such a process depends on the position of the trap energy level inside the bandgap, since upon successful recombination a trap needs to capture an electron from the conduction band and a hole from the valence band. Therefore, the recombination rate becomes maximum for a trap located in the middle of the bandgap. Hence, the ideality factor of a diode is equal to one, if the current is limited by recombination in

the bulk and equal to two if the current is limited by recombination in the space charge region. Values between one and two may also be obtained, since the two effects may coexist. In practise, however, higher values ($n > 2$) may be found experimentally. For these cases, the single junction diode equation with resistances (equation 2.9) is too simple to describe the real device, and the model is therefore not strictly appropriate. It is generally assumed that such deviations are caused by the complexity of the polycrystalline materials e.g. grain to grain differences in diode behaviour, complex interactions of the grain boundary electric fields with those of the p-n junction, or else grain boundary conductive pathways. Additionally, for the case of CdTe, the contacts are invariably non-Ohmic, but even use of a two-diode model is insufficient to allow physically meaningful values of n to be extracted from experimental data. Overall, values of $n > 2$ are not physical, but they are nevertheless frequently reported in the literature without further justification.

Multi-step tunnelling: One of the mechanisms that can limit current flow in the depletion region is multi-step tunnelling, as shown in the schematic diagram in Fig 2.5a. In such a process, electrons can tunnel through the bandgap using a uniform distribution of localised energy states. A mathematical treatment of the phenomena allows eq. 2.10 to be written to describe the forward bias characteristic J-V response of this process as described in refs^{16–18}:

$$J_{MST} = J'_0 e^{BT} e^{AV} = J_0 e^{AV}, \quad \text{Eq. 2.10}$$

where J'_0 and B are constants, $J_0 = J'_0 e^{BT}$ is the saturation current, T is the temperature, A is the slope of $\ln J_{MST} - V$ and V is the applied voltage. Although in this process there is no physical meaning to $n = \frac{q}{AkT}$ ($n \gg 1$), the temperature dependence of A and n are

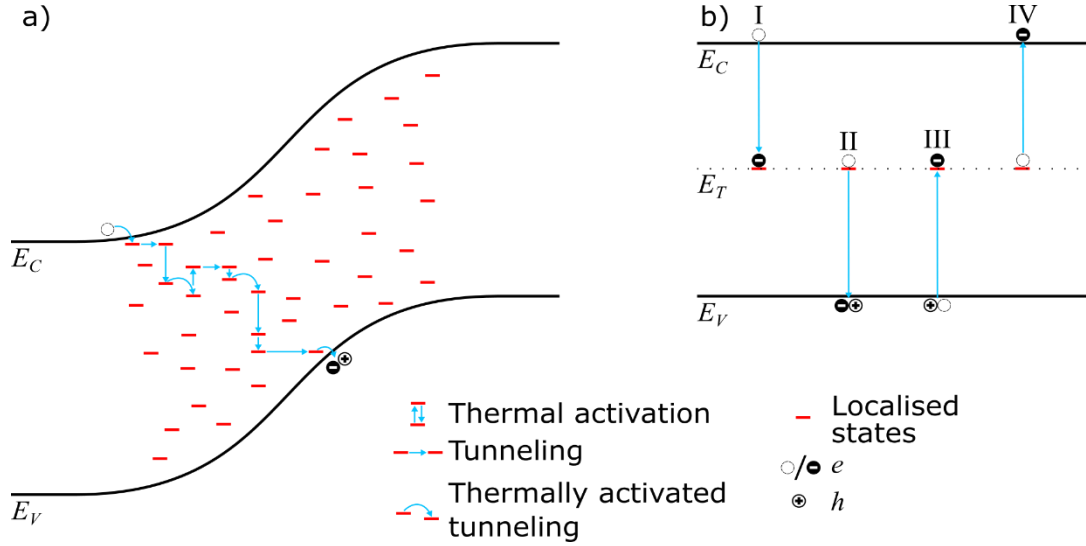


Fig. 2.5 Charge carrier transport limiting effects multi-step tunnelling (a) and Shockley-Read-Hall (b) mechanisms. I-IV: trap-assisted electron capture (I), hole capture (II), hole emission (III) and electron emission (IV).

usually used to test/validate the multi-step tunnelling mechanism. The number of tunnelling steps involved in such a process can be calculated as follows^{19,20}:

$$R = \frac{m_n \epsilon_p}{N_A} \left(\frac{\pi}{4\hbar A} \right)^2 \left(1 + \frac{\epsilon_p N_A}{\epsilon_n N_D} \right)^2 \quad \text{Eq. 2.11}$$

$$R \approx \frac{m_n \epsilon_p}{N_A} \left(\frac{\pi}{4\hbar A} \right)^2, N_D \gg N_A, \quad \text{Eq. 2.12}$$

where m_n is the electron effective mass and \hbar the reduced Planck's constant. This analysis allows evaluation of experimental $J - V - T$ data to check with consistency with the multi-step tunnelling process.

J-V-T measurements and Shockley-Read-Hall recombination: Carrier flow through the junction may be influenced by trapping and recombination processes that occur at localised states within the bandgap. In particular, for an acceptor-type trap the four thermally activated/de-activated distinct processes that are shown in Fig 2.5b (I – IV) are:

- capture of an electron that undergoes relaxation from the conduction band to the trap (I),
- capture of a hole in the valence band via recombination by releasing a trapped electron to the valence band (II),
- emission of a hole into the valence band by trapping a thermally excited electron from the valence band (III) and
- emission of a trapped electron into the conduction band via excitation (IV).

The highest recombination probability via traps is observed for $E_T = \frac{E_g}{2}$ and in this case the diode ideality factor becomes $n = 2$ (see Ref.¹). Assuming that the R_S and R_{SH} terms are negligible, the J - V response is described as:

$$J_{SRH} \approx J_0 e^{qV/nkT}, \quad \text{Eq. 2.13}$$

where n can be calculated from the slope of $\ln J_{SRH} - V$. For the case of mid-gap trap states $n = 2$. However, as mentioned above, in J - V - T measurements, n is often found to be much higher than 2. For such cases, its value and its temperature-dependence are used instead in the literature as a ‘fingerprint’ to identify the ongoing carrier transport mechanism that takes place in the solar cell device. However, since values of $n > 2$ have no physical significance (see above), this use of the temperature dependence of high value of n has developed empirically and is not scientifically robust. Lastly, J_0 can be determined from the intercept of $\ln J_{SRH} - V$ and its temperature dependence is described as:

$$J_0 = J'_0 e^{\Delta E/nkT}, \quad \text{Eq. 2.14}$$

where ΔE is the activation energy.

2.2.3.3 Solar cell parameters

The key parameters in the characterisation of the PV performance of solar cells are the short circuit current density J_{SC} , the open circuit voltage V_{OC} , the maximum power point (MPP), the fill factor FF and the power conversion efficiency η . These parameters are extracted from the J - V characteristic curve under illumination shown in Fig 2.6. This measurement is performed in a solar simulator under standard test conditions, i.e. 1000 W/m², AM1.5 spectrum²¹ at 25°C.

The short circuit current is the current that flows in the external circuit when the solar cell electrodes are short circuited and depends on the intensity of the incident photons and the optical properties of the solar cell (absorption and reflection).

The open circuit voltage is the value of the applied voltage for which no current flows through the external circuit and it is the maximum voltage that the device can deliver. Essentially, it is the forward bias, at which the photogenerated and the dark current cancel each other out. It depends on the photogenerated current density and can be determined using Eq. 2.8 as follows:

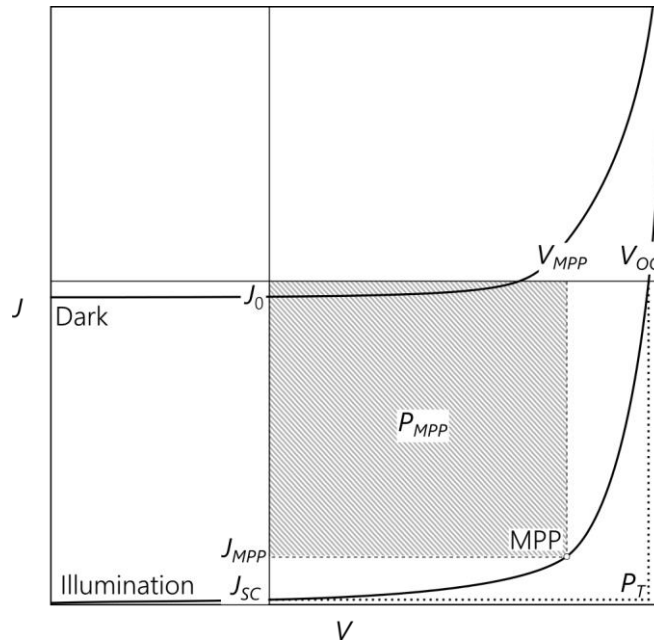


Fig. 2.6 Typical light and dark J - V curves for a solar cell device.

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{J_L}{J_0} + 1 \right) \quad \text{Eq. 2.15}$$

The maximum power point is the point in the J - V curve, where the current-voltage product had the highest value, i.e. maximum solar cell power output, while the fill factor is determined by the ratio of the maximum power with the J_{sc} and V_{oc} product:

$$FF = \frac{J_{MPP} V_{MPP}}{J_{sc} V_{oc}} \quad \text{Eq. 2.16}$$

In real devices, FF is significantly influenced by the series and shunt resistance of the solar cell. Finally, the power conversion efficiency is calculated as follows:

$$\eta = \frac{J_{sc} V_{oc} FF}{I_{in}}, \quad \text{Eq. 2.17}$$

where $I_{in} = 1000 \text{ W/m}^2$ is the irradiance under standard conditions.

2.2.4 Shockley-Queisser limit

One of the fundamental loss mechanisms in solar cells is thermalisation, where the excess energy of hot carriers is wasted by relaxation to the conduction band edge. Because of this, the maximum power conversion efficiency of solar cells is directly related to the bandgap energy of the absorber layer and the intensity of the absorbed photons. This upper limit of the PV performance of single-junction solar cells is described by the Shockley-Queisser (S-Q) limit²², which was introduced in 1961 and remains one of the most fundamental tools in the field of photovoltaics. It is based on the principle of detailed balance and it is determined by calculating the generated electrical energy per incident photon. For the calculation, a single junction solar cell comprising a single absorber layer is illuminated by the non-concentrated emission of

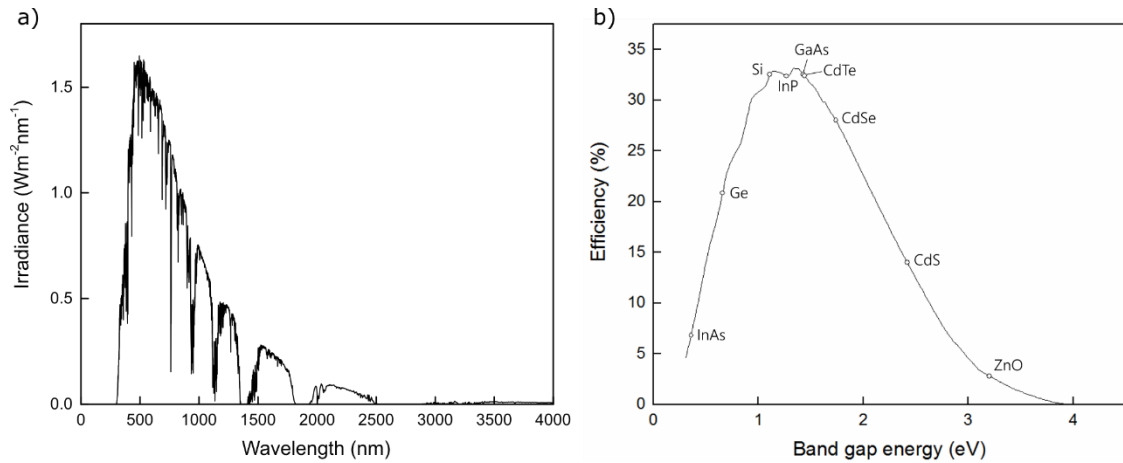


Fig. 2.7 a) The reference AM1.5 spectrum plotted from the ASTM G173-03 tables²¹. b) The Shockley-Queisser limit of single junction solar cells at 25°C illuminated by the ASTM G173-03 spectral irradiance (Rühle²⁴). The bandgap of semiconductor materials that are commonly used in photovoltaics are marked.

a black body at 6000K (the Sun). Today, however, the evaluation of the performance of solar cells is carried out using the AM1.5 spectral irradiance (Fig 2.7a), which is the standard reference solar spectrum²¹. It corresponds approximately to a black body radiation at 5800K attenuated by Earth's atmosphere²³ at 37° tilt toward the equator, facing the sun. The modified S-Q limit is plotted in Fig 2.7b using tabulated values presented by Rühle²⁴. Since V_{OC} relates to V_{bi} and E_g , higher values are expected at wide bandgap materials. However, because the photon intensity is not constant across the whole spectrum and is wavelength-dependent, less photons will be absorbed in materials with high bandgap values. Therefore, according to the modified S-Q limit, the maximum power conversion efficiency is 33.16% for a semiconductor with a 1.34 eV bandgap. However, multi-junction solar cells, up/down conversion materials, multiple electron-hole pair generation, optical concentration and quantum confinement effects can lead to efficiencies that exceed the S-Q limit.

2.2.5 Losses in real solar cell devices

2.2.5.1 Optical losses

The PV parameters of a solar cell and, mainly, the J_{SC} depend on the number of photons that are absorbed in the device and successfully converted to electrons. However, optical losses can occur because of parasitic absorption in layers that do not generate electron-hole pairs, reflections at the various device interfaces or light that escapes the device without being absorbed. Therefore, the absorbance, transmittance and reflectance of the individual solar cell components are crucial for optimal PV performance.

Parasitic absorption in the front-most layers of a solar cell can often lead to performance shortfalls. In ‘superstrate’ CdTe/CdS devices for example, photons with sufficient energy have a high probability to be absorbed in the CdS window layer due to the high absorption coefficient of CdS. However, because $N_D \gg N_A$ the depletion region is solely in the CdTe and hole recombination occurs before they are successfully transported to the depletion region. Parasitic photon absorption can also occur in the high resistive transparent layer, such as ZnO in the case of CdTe/CdS solar cells, and in the front transparent conducting oxide (TCO). Furthermore, photons that are absorbed deep in the p -type layer at a distance greater than the minority diffusion length may also recombine before reaching the depletion region. Lastly, absorption losses can occur due to the finite thickness and the absorption coefficient of the absorber layer.

As shown in Section 2.2.2, photons with energies lower than the bandgap energy of the absorber layer are not absorbed, while thermalisation losses occur when hot carriers are generated upon absorption of high-energy photons. The thermalisation process increases the temperature of the device, which leads to higher intrinsic carrier concentrations. This potentially results in higher reverse saturation currents, longer minority carrier diffusion lengths and V_{OC} losses²⁵.

Optical losses can also occur due to reflection of photons at the front surface or at the various interfaces of the device, which can guide the light outside of the device and escape absorption. Finally, shading losses can occur in the front contacts by preventing light from entering the device²⁶. Optical losses can be limited by the inclusion of anti-reflection layers or by thinning down the layers that do not contribute to the photocurrent.

2.2.5.2 Recombination losses

Radiative or non-radiative carrier recombination is a process where electrons and holes are annihilated before they can be successfully collected leading to potential J_{SC} losses. Typically, recombination can occur in the bulk, at the depletion region or at the free surfaces and interfaces of a solar cell device. Apart from the losses in photocurrent, recombination has an adverse impact in the open circuit voltage. By definition, V_{OC} is the voltage at which the forward bias diffusion current becomes equal and opposite to the J_{SC} . Upon recombination, however, the injected minority carriers vanish, which leads to more carriers diffusing across the junction. Therefore, at high recombination rates, the forward bias diffusion current cancels out the J_{SC} at lower V_{OC} values. This can be further understood by the J - V junction response (Eq. 2.7). The reverse saturation current, J_0 , is a measure of the recombination in a device and increases with recombination rate. Therefore, for the same voltage, higher J_0 values lead to higher forward bias diffusion current.

Recombination losses usually occur due to impurities, defects and dangling bonds which introduce carrier traps. Therefore, passivation and chemical treatment of surfaces and interfaces, heavy doping and the use of single crystals or high-purity materials can increase the carrier diffusion lengths and decrease the recombination losses²⁷.

2.2.5.3 Resistive losses

In Section 2.2.3.1, it was shown that current, voltage and fill factor losses occur in non-ideal solar cell devices due to the effect of the series and shunt resistances. The series resistance of a solar cell comprises several components, such as the bulk resistances of the various device layers including the front and back contacts and the contact resistance between semiconductor-semiconductor or semiconductor-metal interfaces. In order to illustrate the main effects, J - V curves were simulated for solar cells having varied R_S and R_{SH} values using a Poisson solver package dedicated to thin film solar cell devices (SCAPS)²⁸. Fig 2.8a shows typical J - V curves for increasing R_S values. High R_S , mainly, affects the FF of the solar cell by decreasing the output current near the V_{OC} (Eq. 2.9), but may also lead to a decrease in J_{SC} for very high values. The effect of R_S scales with illumination intensity and the photogenerated current²⁹. R_S can be determined by the inverse of the slope of the J - V curve close to the V_{OC} .

The shunt resistance of a solar cell device is a measurement of the leakage current due to shunting pathways. Current leakage paths in solar cells can occur around cut edges, near crystal defects and contaminants or through pinholes. The impact of R_{SH} on the PV performance is shown in Fig 2.8b, where increasing R_{SH} values lead to FF losses by reducing the amount of current that flow through the junction and in extreme cases acts

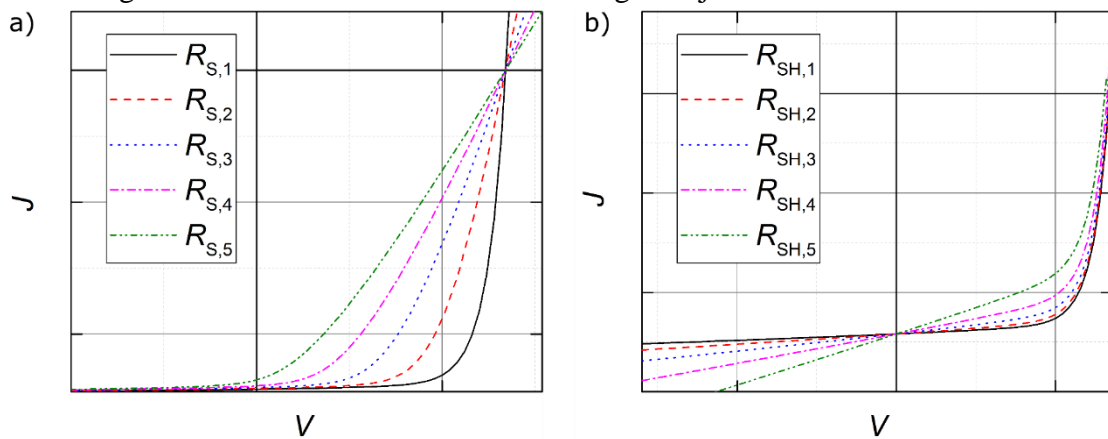


Fig. 2.8 SCAPS²⁸ simulated J - V curves for varying R_S (a) and R_{SH} (b) values. Increasing R_S results in FF losses and for very high values in J_{SC} losses.

to reduce V_{OC} . The effect of R_{SH} becomes more severe at low-intensity illumination, since the photogenerated current is low. R_{SH} can be determined by the inverse of the slope of the J - V curve close to the J_{SC} .

2.2.5.4 Metal-semiconductor interface losses

When a metal and a semiconductor are brought in contact, a potential barrier can be formed at the junction depending on the energy mismatch between the Fermi levels. Thus, an Ohmic or a rectifying contact (Schottky junction) can be formed. The band structures of the two contact types between a metal and a p -semiconductor are shown in Fig 2.9. While in the Ohmic contact, holes can flow in or out of the semiconductor with minimal contact losses, the potential barrier in the rectifying contact reduces the hole extraction efficiency. The rectifying back-contact can be modelled as a second diode of opposite polarity connected in series to the main junction. This causes a characteristic ‘rollover’ in the J - V curve at high forward bias. Such effects are typical in CdTe solar cells⁴, because of the high work function of p -CdTe. The barrier height

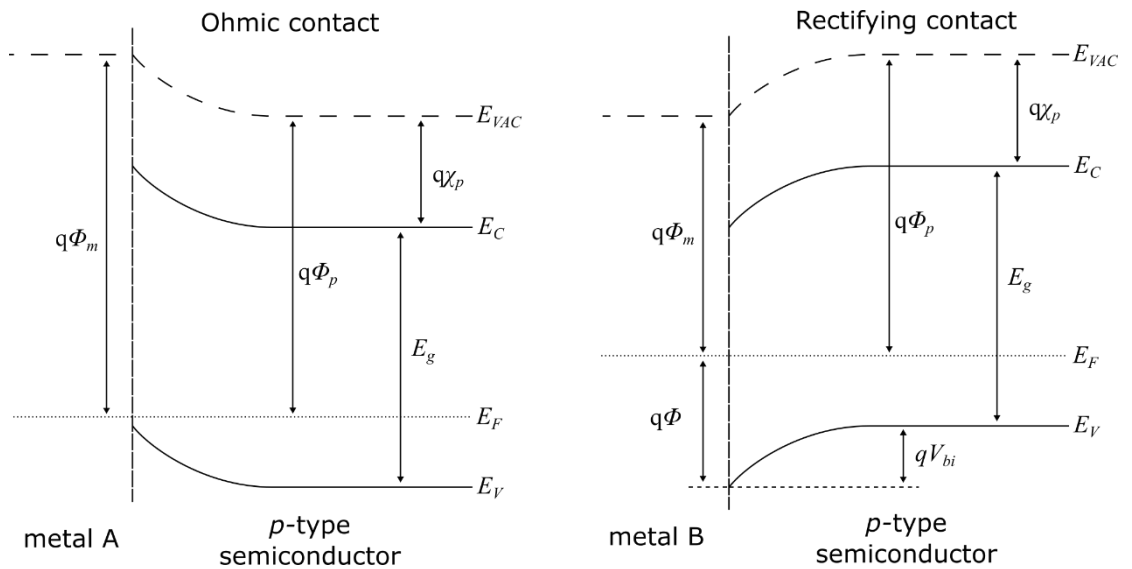


Fig. 2.9 Energy diagrams of an Ohmic and a rectifying metal – p -semiconductor contact. The lower work function of metal B (right) causes a downward band bending, which results in the formation of a hole barrier. Rectifying back-contacts are typical in CdTe/CdS solar cells due to the high work function of p -CdTe.

can be lowered by forming intermixed layers or by incorporating buffer layers⁵. Alternatively, a tunnel contact can be formed by heavy doping of the semiconductor, which narrows the depletion region at the metal-semiconductor interface increasing the tunnelling probability of carriers across the barrier. In addition to this, heavy doping of the back surface or the use of appropriate buffer layers may also reduce the flow of minority carriers, i.e. electrons from the CdTe layer flowing to the back contact, which can result in V_{OC} improvements³⁰.

2.3 CdTe solar cell device technology

2.3.1 *Material properties of CdTe*

CdTe is a II-VI semiconductor that can crystallise both in the zincblende and in the wurtzite structure³¹, since the two phases have similar energies. Although CdTe usually adopts the zincblende symmetry due to enhanced stability³², it is susceptible to stacking faults, dislocations and twinning effects^{33,34}.

Due to its remarkably high absorption coefficient^{35,36}, CdTe films with a thickness of few micrometres are able to capture ~ 90% of the incident radiation³⁷. Furthermore, CdTe has a direct bandgap of ~ 1.5 eV at room temperature, which enables optimal absorption of the solar spectrum²¹ for PV applications. According to the S-Q limit the maximum theoretical efficiency of CdTe solar cells is 32%. Finally, due to the low thermal expansion coefficient, CdTe solar cells demonstrate enhanced performance stability at high temperatures compared to other solar cell technologies, such as Si^{25,38}.

Some of the typical CdTe deposition techniques are close-spaced sublimation (CSS), sputter deposition, electrochemical deposition (ECD), metal-organic chemical-vapour deposition (MOCVD) and vapour transport deposition. Among these techniques, CSS

is one of the most commonly used, being successfully implemented in commercial production of CdTe PVs.

2.3.2 Device structure

Two typical configurations are used in the development of CdTe-based solar cells, the ‘superstrate’ and the ‘substrate’, with the ‘superstrate’ being the established commercial device configuration. Schematic diagrams of the two device types are shown in Fig 2.10. ‘Superstrate’ cells are developed on rigid glass substrates in the following layer sequence: TCO/CdS/CdTe/Au (back contact). This offers more control for treatment of the back surface of the device in order to overcome the back-contact barrier effects⁴ by post-growth chemical etching, doping or inclusion of buffer layers. On the contrary, an inverted stacking sequence is used in ‘substrate’ cells: CdTe/CdS/TCO (front contact). This limits the back-contact processing routes, but enables the use of lighter, thinner, flexible and more robust metallic or plastic substrates. The key features of the main device components are discussed below.

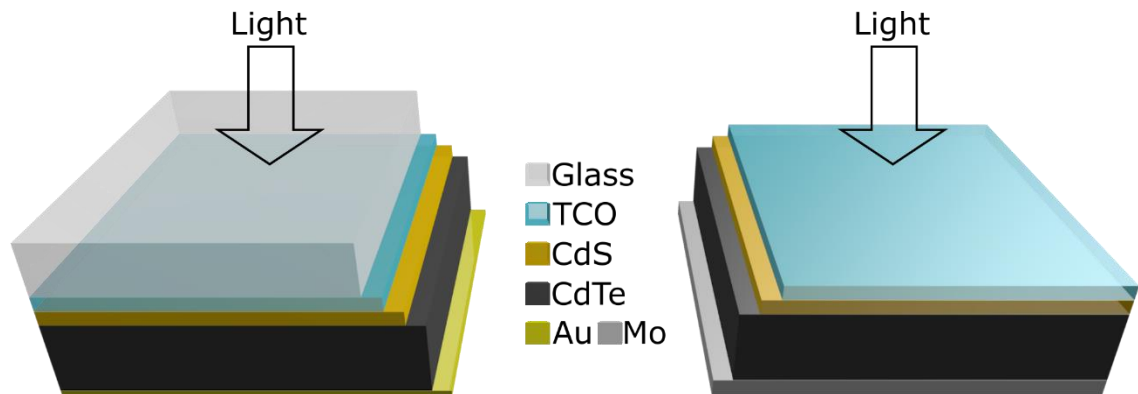


Fig. 2.10 Schematic diagrams of typical CdTe solar cells adopting the ‘superstrate’ (left) and ‘substrate’ (right) configuration. While ‘superstrate’ cells are developed on rigid glass substrates offering more control over the back-contact interface, in ‘substrate’ devices an inverted layer stacking sequence is used, which enables the use of lighter, thinner and flexible metallic or plastic substrates.

2.3.2.1 *Superstrates and substrates*

In the ‘superstrate’ configuration, the various layers are developed on soda-lime glass usually, while borosilicate glass can also be used to limit diffusion of impurities. Such glass superstrates have very high light transmittance ($> 80\%$) and can withstand the processing temperatures during growth. Often, pre-coated glass superstrates with TCO films and HRT layers, such as Pilkington’s TEC glass series with optimised thermal, electrical and optical properties for PV applications are used. On the contrary, a wider range of materials can be used in the ‘substrate’ cells, since they are not required to be transparent. Thus, cheaper materials, such as metal or polymer foils⁵ can be used.

2.3.2.2 *Front contacts*

TCO layers³⁹ such as Al-doped ZnO, SnO₂, F-doped SnO₂ (FTO) and In₂O₃/SnO₂ (ITO) are some of the materials that are commonly used in CdTe solar cells as front contacts. They act as electrodes with a sheet resistance of, usually, a few Ω/\square , in order to extract carriers from the solar cell device, while their wide bandgap allows high transmittance in the visible regime. Usually, TCOs have a thickness of few hundreds of nanometres and are deposited by the sputtering deposition technique. The reader is referred to Ref.⁴⁰ for a comprehensive review of TCOs for PV applications.

2.3.2.3 *CdS window layer*

Cadmium sulphide is one of the most common window layer materials in PV technology⁴¹ and specifically in CdTe solar cells. It crystallises in the wurtzite symmetry and has a relatively wide bandgap of 2.4 eV⁴², high absorption coefficient and high doping density⁴³ ($> 10^{17} \text{ cm}^{-3}$). Moreover, a good type-I band alignment between the CdTe and CdS layer has been reported^{44,45}. In CdTe/CdS solar cells though, due to the doping imbalance between the *n*-CdS and *p*-CdTe layers, the depletion region is one sided and solely located in the CdTe layer. Thus, light absorption in the CdS layer

is unfavourable, since the photogenerated minority carriers recombine before reaching the depletion region and do not contribute in the photocurrent. One way to limit current losses due to parasitic absorption is to thin down the CdS layer below 100 nm, which enables higher transmittance of light. For this purpose, CdS is usually deposited by means of sputtering⁴⁶ or chemical bath deposition⁴⁷ techniques, which produce very smooth and uniform films. However, in very thin films the formation of pinholes can lead to leakage paths and V_{OC} shortfalls. Alternatively, CdS:O window layers are used, which are reported to have a wider bandgap^{48,49}. Finally, CdTe solar cells comprising CdS:O/CdSe window bi-layers have been reported⁵⁰ with enhanced current collection.

Due to a high lattice mismatch between the CdS and CdTe layers, dislocations at the interface may act as recombination traps with a detrimental effect on PV performance. During the following development steps, however, interdiffusion of S and Te between the two layers occurs at high temperatures and a $Cd_xS_{1-x}Te$ intermixed layer is formed. This acts to increase the junction quality and the overall PV performance. However, extended interdiffusion at high temperatures may have adverse effects. This is because of a) the formation of pinholes in the thin CdS layer, which may lower the V_{OC} and b) enhanced parasitic absorption in the CdS/ $Cd_xS_{1-x}Te$ layers due to the incorporation of Te which reduces the bandgap energy⁵¹.

2.3.2.4 CdTe absorber layer

p-CdTe is the primary absorption and photoconversion layer in CdTe/CdS solar cells with a typical thickness as low as $\sim 2 - 6 \mu m$, which contributes significantly to the low manufacturing costs. Usually, polycrystalline CdTe films are deposited by means of sputtering⁵², CSS⁵³ or MOCVD⁵⁴. Although solar cell devices comprising single-crystal CdTe layers demonstrate exceptional V_{OC} values⁵⁵⁻⁵⁷, their overall PV performance is lower compared to that of polycrystalline CdTe devices. While the low performance of

single-crystal devices requires further investigation and is beyond the scope of this work, the performance of polycrystalline devices depends strongly on the grain size, shape and the number of grain boundaries⁵⁸. However, their role can be counter-intuitive in some cases. Usually, grain boundaries are thought to have adverse effects by: a) increasing the series resistance due to energy barriers and enhanced carrier scattering, b) introducing recombination centres due to dangling bonds or segregation of impurities and c) acting as shunting pathways. While such phenomena may take place in polycrystalline CdTe layers with a detrimental effect on PV performance, grains and grain boundaries may, actually, reduce recombination. In particular, enhanced electron transport was observed in grain boundaries, whilst grains acted as transport media for the holes separating the carrier diffusion pathways. An additional effect of the grain boundaries is the successful diffusion of Cl during the Cl treatment (Section 2.3.3), which enhances the *p*-type doping. For further information on the role of grain boundaries, the reader is referred to the comprehensive review by Major⁵⁹.

2.3.2.5 Back contacts

Carrier extraction in CdTe solar cells is often found to be challenging due to the formation of a Schottky barrier at the CdTe-back contact interface. This is because the scarcity of contacting materials with high enough work function to match that of *p*-CdTe. In order to lower the back-contact barrier height and its effects⁴ the use of chemical etching, doping or inclusion of buffer layers⁵ has been reported. Heavy doping of semiconductor at the interface narrows the depletion region at the metal-semiconductor junction increasing the tunnelling probability of carriers across the barrier. Au is one of the most commonly used back-contact materials in ‘superstrate’ devices^{60–63}, while Mo in ‘substrate’ devices^{5,64–66}.

2.3.3 Cl treatment

Cl treatment of CdTe solar cells is a key manufacturing process which influences a) the doping of the CdTe thin film⁶⁷, b) formation of the p - n junction^{68,69}, c) grain boundary passivation⁷⁰, d) recrystallisation and grain growth^{71,72}. These effects have a beneficial impact on the overall PV performance of CdTe devices⁷³. Doping CdTe with Cl involves two counteracting processes: a) substitution of a Te atoms with Cl (Cl_{Te}), which act as a shallow donors and b) the formation of Cd vacancies (V_{Cd}), which act as double acceptors. Thus, the formation of the acceptor complex $(V_{\text{Cd}}\text{-Cl}_{\text{Te}})^{-1}$, known as A-centre, possibly leads to the p -doping of CdTe. The most commonly used process involves the diffusion of Cl into the CdTe bulk from a CdCl_2 layer or solution at high temperatures $\sim 400^\circ\text{C}$. Since CdCl_2 is toxic and highly soluble in water, special handling and waste disposal procedures are required, which increases the environmental hazards and production costs. Nevertheless, in this work, instead of the standard CdCl_2 treatment, a novel MgCl_2 treatment process⁶³ was employed, which is non-toxic and has the potential to reduce manufacturing costs

2.3.4 Progress review of the CdTe PV performance

Due to its perfectly matched to the solar spectrum direct bandgap and its high absorption coefficient, CdTe has been established as one of the best candidate materials for PV applications since the 1950s. The early industrial leaders in CdTe PV manufacturing were General Electric, Kodak, Monosolar, Matsushita, and AMETEK. One of the first CdTe solar cells was reported in 1959 by Rappaport⁷⁴ with a peak efficiency of 2.1%. In 1969, Adirovich⁷⁵ first demonstrated the fabrication of the CdTe/CdS ‘superstrate’ solar cells and, three years later, Bonnet and Rabbenhorst⁷⁶ reported efficiencies of up to 6% using a graded bandgap $\text{CdS}_x\text{Te}_{1-x}$ solar cell. The deposition of CdTe by means of close space sublimation was first reported by Kodak⁷⁷ in 1980 with PV devices

achieving ~ 10% conversion efficiency. Further major performance enhancements were reported by the University of South Florida⁷⁸ in 1993 with the record efficiency of CdTe solar cells increasing to ~ 16%. This was achieved by incorporating a thin SnO₂ buffer layer between the TCO and the CdS layers, which allowed the thinning of the CdS layer and the reduction of the optical losses. However, the technological progress of CdTe PVs in the next years was slow. It was not until 20 years later, with a series of performance enhancements reported by First Solar and General Electrics that the record efficiency climbed to 22.1%¹⁰. The reader is referred to Refs.^{79–81} for more information on the progress of the CdTe solar cell technology.

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3 Nanowire growth and nanowire-based solar cells

3.1 Introduction

In this Chapter, the growth of semiconductor nanowires and the development of nanowire-based solar cells is reviewed. In Section 3.2, the various top-down and bottom-up synthetic approaches for the growth of nanowires are described. An emphasis on the bottom-up selective area and metal-catalysed VLS growth methods has been given, since these two techniques were employed in this work to test the growth of CdTe nanowires using CSS deposition (Chapter 5). In addition to this, a review of the literature regarding the growth of CdTe nanowires is given in Section 3.2.3. Next, the most common NW solar cell device configurations and their potential advantages over planar devices are discussed in Section 3.3. Other NW solar cell device configurations do exist, such as the nanowire dye-sensitised solar cells, but are not included, since they do not relate to the scope of this work. Although NW devices are, theoretically, superior over traditional bulk or thin-film devices, their PV performance is still significantly lower with the main limiting factors being discussed in Section 3.3.3. Finally, the up-to-date state-of-the-art NW PV devices are reviewed in Section

3.4.1, while a literature review with a focus on CdTe-related NW-based devices is given in Section 3.4.2.

3.2 Semiconductor nanowire growth techniques

3.2.1 Top-down approach

In a typical top-down growth process¹, nanowires are fabricated by removing material away from a bulk material. The bulk material is masked and, subsequently, patterned using either lithography², nanoimprint³ or particles⁴ and nanowires are developed by selectively etching the redundant material. Alternatively, nanowires can be developed using focused-ion-beam milling^{5,6}. Compared to the bottom-up, the top-down approach offers better and complete control over the geometry, alignment, position and size of the nanowires. Nevertheless, some of the benefits of the bottom-up approach, such as the ability to accommodate strain in lattice mismatched materials, single crystal growth and material savings are largely lost. The development of high quality single-crystal nanowires using the top-down would require single-crystal high quality bulk material or epilayers adding significantly to the process costs. Furthermore, in lithography-assisted methods, the process is limited by the instruments resolution and additional costs are added. Finally, top-down methods have lower throughput and are less scalable, making them unfavourable for industrial applications.

3.2.2 Bottom-up approach

In the bottom-up approach, nanowires are grown by additive processes. This requires the conditioning of the growth environment so that nanowire growth becomes more favourable over bulk 2-dimensional growth, i.e. growth is catalysed at the NW sites. Free standing nanowires^{7,8} and nanowires grown on substrates⁹ can be obtained using a wide range of methods. Some of the most common are the catalyst-assisted vapour-

liquid-solid^{9,10}, selective area¹¹, catalyst-assisted selective area¹¹ and self-assembly¹². In this work, the gas-phase vapour-liquid-solid and selective area methods were tested for the growth of CdTe nanowires and are discussed below. The reader is referred to Refs.^{13–15} for a comprehensive review of nanowire growth including additional synthesis methods.

3.2.2.1 Selective area gas-phase NW growth

This growth method uses patterned substrates with areas that define the nanowire growth locations. The patterned layers are usually oxides with holes exposing the underlying substrate, which typically is oriented along preferred growth orientations. Thus, upon exposure to a semiconductor vapour or precursors, nanowire growth is promoted over bulk growth due to surface energy differences and the rapid epitaxial growth of certain crystal facets¹⁶. Nanowire growth can be further promoted by adding catalyst particles located in the patterned areas¹⁷, but this can introduce undesirable contaminants.

Several techniques¹⁸ can be used for substrate patterning: electron beam lithography^{19–21}, UV lithography²², nanosphere lithography^{23,24} and nanoimprint lithography^{3,25,26}. Although the nanoimprint and nanosphere lithography techniques offer higher-throughput and are cheaper than the electron beam lithography, additional cleaning steps may be required in order to remove organic residues which may interfere with nanowire growth²⁵. Overall, selective area NW growth provides superb control over the location, the size and the pitch of the nanowires, producing very homogeneous NW arrays. Although for certain applications this can be advantageous over other methods, NW properties, such as optical absorption is not always limited by the homogeneity of the NW array²³. For further details on the various selective area methods, the reader is referred to the comprehensive review by Tomioka¹³.

3.2.2.2 Catalyst-assisted vapour-liquid-solid NW growth

This technique is one of the most widely used and successful methods for the growth of nanowires. It employs liquid catalyst droplets, which act as nucleation centres promoting nanowire growth and it was first demonstrated by Wagner and Ellis⁹ in 1964 for the growth of Si ‘whiskers’. The fundamental aspects of VLS growth were studied in more detail by Givargizov²⁷ in 1975 using Si ‘whiskers’ grown by chemical vapour deposition. The growth mechanism can be explained as follows: the constituent atoms of the nanowires, supplied in the *vapour* phase, diffuse into the *liquid* catalyst droplets and upon supersaturation *solid* monolayers precipitate. Nanowire growth using solid-state catalysts is also possible^{28,29}, but it is slower with lower nanowire aspect ratios and lesser crystal quality. Unidirectional nanowire growth is achieved by preferential nucleation of the growth species at the liquid-solid interface, a process which is governed by the growth conditions³⁰. Typically, nanowires grown by this technique bear spherical particles at their tips, which are the catalyst remnants from the growth process.

The most common catalyst used in the VLS growth of Si³¹, Ge³², ZnO³³, III-V³⁴ and II-VI³⁵⁻³⁹ nanowires is Au. Nevertheless, other metals, such as Al⁴⁰, Sn⁴¹, In⁴², Sb⁴³, Bi⁴⁴, Ga⁴⁵, Fe⁴⁶, Co⁴⁷, Cu⁴⁸, Ni⁴⁹, Pd⁵⁰, Ge⁵¹ and Pt⁵² have also been used successfully. According to Dubrovskii⁵³, the main catalyst requirements at the growth conditions are: (1) Formation of a liquid catalyst-semiconductor alloy. (2) Very low or zero solubility in the solid phase and high solubility in the liquid phase. (3) High catalytic performance in the adsorption-desorption and diffusion processes. (4) High liquid surface energy in order to reduce wetting and instability phenomena at the nanowire-droplet interface. Furthermore, ideally, the catalyst should be chemically inert and non-volatile in order to limit formation of solids and evaporation of the catalyst during growth. Finally,

catalyst oxidation during growth can be detrimental to the process. Thus, when catalysts that are susceptible to oxidation are used, an oxygen-free or reducing growth atmosphere is required⁵⁴.

Fig. 3.1a shows the main stages during the Au-catalysed VLS growth of Si nanowires. The Au-Si binary system⁵⁵ was chosen as an example due to its simplicity. In the first stage (I), catalysts are formed on the substrate's surface using colloids, aerosols or thermal evaporation⁵⁶⁻⁵⁸. Deposition of catalysts in a patterned fashion is also possible using lithographic techniques, which offers better control over the NW array characteristics. Next, the catalysts are heated inside the growth chamber until they melt (II). During this stage, atoms from the substrate may diffuse into the catalyst and form an alloy. In the next stage (III), the Si vapour is introduced to the chamber. Si adatoms arrive into the liquid catalyst either by direct impingement or by surface diffusion increasing the Si content. In the example of Fig. 3.1b, at a growth temperature of 900°C, the liquidus line is crossed when the Si content is approaching ~ 42 at%. At this point, if the required conditions are met, further incorporation of Si is possible, which results in the supersaturation of the catalyst. Ultimately, since this state is thermodynamically unstable, Si precipitates and crystallises at the liquid-solid interface. At this point, the catalyst becomes depleted of solid Si and the Si content drops back to ~ 42 at% (liquidus line). Eventually, if a constant supply of Si vapour is maintained, nucleation at the liquid-solid interface proceeds continuously and steady state NW growth (IV) occurs. During this stage, since nanowires grow at the solid-liquid interface in a layer-by-layer manner, a constant nanowire diameter is expected if the growth area, i.e. the droplet-nanowire area remains the same. Although this is often the case, gradual volume reduction of the catalyst and nanowire shrinking may occur during growth due to instability, diffusion, incorporation, evaporation or reaction phenomena^{40,59}.

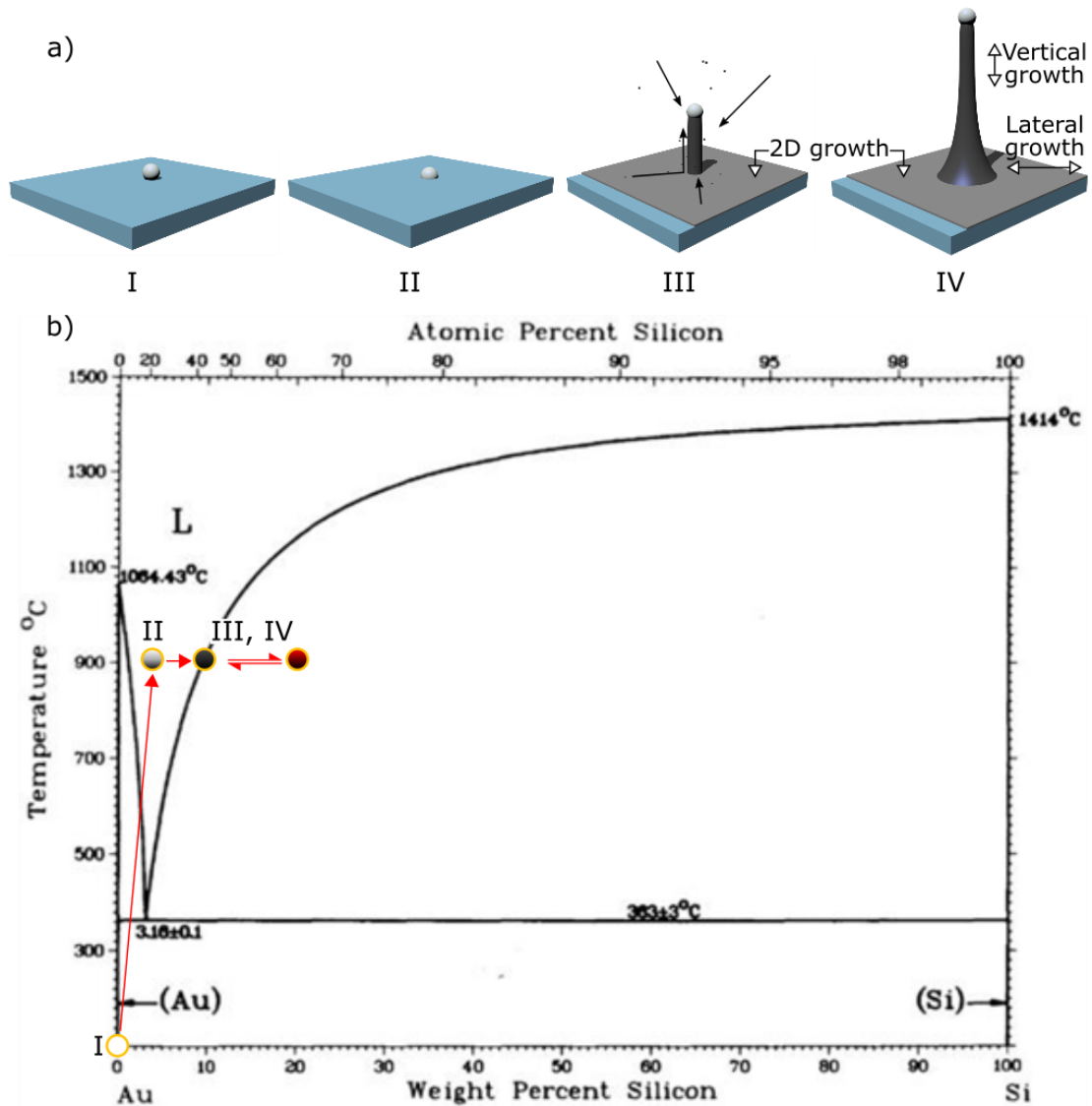


Fig. 3.1 a) Schematic of the main VLS growth stages: catalyst formation (I), catalyst melt and alloying (II), NW growth initiation (III) and NW steady growth (IV). Although nanowire growth is energetically more favourable over bulk growth, thin film deposition is often observed as shown in III and IV. b) Modified Au-Si binary phase diagram⁵⁵ illustrating the compositional evolution of the catalyst during VLS growth. In this example, a growth temperature of 900°C was chosen for a better visualisation of the process. Usually, however, growth temperatures are much lower. (diagram reproduced from Ref.⁵⁵).

Furthermore, in nanowires with lengths exceeding the surface diffusion length of the adatoms, uncatalyzed vapour – solid growth occurs on the nanowire sidewalls^{27,60} and results in lateral growth and tapering phenomena. Steady state NW growth terminates when the vapour deposition is stopped. Often, however, nanowire growth can continue

due to the finite time required until the catalyst becomes fully depleted. During this time, the catalyst volume decreases as the semiconductor atoms precipitate out and a characteristic tapering is observed at the nanowire tip. This is known as the ‘reservoir’ effect and has been thoroughly investigated^{61,62} due to its impact on the formation of abrupt interfaces in axial nanowire heterostructures grown by the VLS method. Its strength scales with the semiconductor solubility in the liquid catalyst.

3.2.3 Review on the growth of CdTe nanowires

In this section, the typical characteristics of CdTe nanowires and a summary of selected reports on the growth of CdTe nanowires with a focus on PV applications are presented.

3.2.3.1 CdTe nanowire characteristics

The majority of CdTe nanowires grown in a bottom-up fashion are single crystalline structures and, typically, occur in the zincblende symmetry^{63–66} along the [111] direction. However, kinks that may occur during growth, can shift the growth along other directions, such as the [100]⁶⁷. The growth of wurtzite CdTe nanowire has been demonstrated by Neretina *et al*⁶⁸, while Luo⁶⁹ has reported the growth of both zincblende and wurtzite structures using sputtering deposition. Although wurtzite CdTe is less stable than the zincblende in the bulk⁷⁰, the additional degree of freedom in nanowire growth can lead to a more stable growth of wurtzite CdTe nanowires. In addition to this, zincblende-wurtzite polytypism⁶⁵ phenomena have been observed in nanowires with adverse effects on their optoelectronic properties^{71–73}. Williams³⁵ have demonstrated the existence of extended defects in Au-catalysed VLS grown CdTe nanowires, such as stacking faults, polytypes and twins.

Photoluminescence measurements of CdTe nanowires have shown evidence of high crystal quality similar to that of single crystal films. Williams³⁵, however, suggested

that impurities from the Au-catalysed VLS growth of CdTe nanowires can contribute to deep level emission, which may be detrimental to PV performance. Furthermore, Huang⁷⁴ findings show blue-shifted and broadened PL spectra of Au-catalysed CVD-grown CdTe nanowires, suggesting residual strain effects in the as-grown CdTe nanowires.

3.2.3.2 Top-down methods

CdTe-based nanostructures in a top-down fashion have been reported by Dang⁷⁵ and Jaroszyński⁷⁵. In both cases, CdTe superlattices were fabricated by molecular beam epitaxy and nanowires were etched using electron beam lithography. Variations between the photoluminescence spectra of nanostructures with varying diameters and thin films of equivalent thicknesses were partly attributed to losses due to surface damage during etching.

3.2.3.3 Solution-phase bottom-up methods

Solution-phase bottom-up grown CdTe nanowires have been reported using various techniques. Among them, one of the most widely used method, compatible with the development of solar cells, is the filling of pores of anodic alumina^{76–79}, polycarbonate^{63,80,81} or nanosphere lithography⁸² templates using electrochemical deposition. This technique offers good control over the NW array geometry by adjusting the pores size, pore-to-pore distance and the thickness of template.

3.2.3.4 Vapour-phase bottom-up methods

One of the most established methods to grow CdTe nanowires is the VLS using CSS^{35,83–85}, CVD^{44,74,86}, ECD⁸⁷, thermal evaporation^{88–94}, MBE^{95–98}, PLD^{68,99} and MOVPE¹⁰⁰. Catalysts that have been successfully used are Au^{35,67,74,83,84,86,88,89,95,96,100}, Au/Ga⁹⁷, Bi^{44,68,90,91,94,101,102} and Bi₂Te₃^{98,99}. Utama *et al*¹⁰³ have demonstrated the self-

catalysed VLS growth of CdTe nanowires on a muscovite mica substrate. In this work, a wide range of catalysts, such as Au, Bi, Bi₂Te₃, Pt, Sb and Sn were tested for the VLS growth of CdTe nanowires using CSS deposition (Chapter 5). Despite the relatively broad literature related to CdTe NW growth, only few employ CdTe CSS deposition. In Refs.^{35,83,84}, Au catalysts were employed, while in Ref.⁸⁵, the co-evaporation of Bi catalysts and the CdTe precursor limited the control over growth.

Uncatalysed vapour-solid growth of CdTe nanowires has been reported by Soshnikov^{104,105} using sputtering deposition of CdTe on a porous SiO₂ layer. Nevertheless, the resulting nanowires had average diameters smaller than 100 nm, since they were limited by the pore dimensions and, thus, they are less favourable for PV applications. Vapour-solid catalyst-free growth of CdTe nanowires was, also, demonstrated by Wang *et al*⁶⁵ using CdTe thermal evaporation on ITO glass substrates. However, the ITO/CdTe contact can hinder the PV performance due to ‘rollover’ effects and act as a limiting factor in the development of a nanowire-based solar cell device.

3.3 Nanowire photovoltaic devices

3.3.1 Nanowire solar cell heterostructures

The main types of nanowire *p-n* heterojunctions that can be used for solar cell applications are shown in Fig. 3.2: a) Axial junctions^{106–109}, where nanowires comprise two (or more) segments of different materials along their axes in a similar stacking sequence as conventional thin film solar cells. b) Substrate junctions^{4,110–113} formed at the interfaces between *p*-type nanowires and an *n*-type substrate. c) Radial junctions^{114–121} formed in *p-n* core-shell nanowires. d) Junctions^{122–124} formed at the interfaces of *p*-

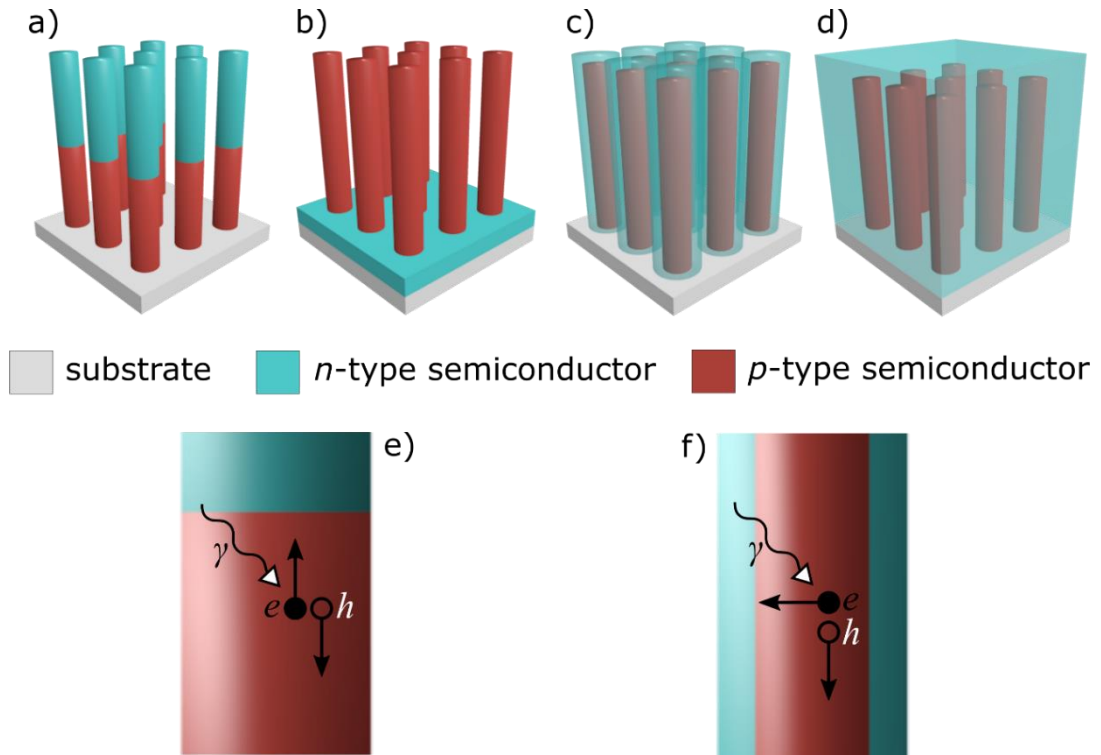


Fig. 3.2 Nanowire heterojunction geometries: a) axial heterojunctions, b) substrate heterojunctions, c) radial heterojunctions and d) embedded heterojunctions. Charge separation in axial (e) and radial (f) junctions

type nanowires embedded in an *n*-type bulk (*embedded* junctions). Some of the differences between the main NW device configurations are discussed below.

Axial and substrate heterostructures behave relatively similarly. Due to strain relaxation effects in nanowires, this architecture enables the development of axially grown tandem nanowire solar cells^{125–127}. Such devices can be, theoretically, advantageous to planar tandem solar cells offering a wider range of material combinations, high material quality, the potential to use lower grade substrate and enhanced optical properties. In addition to this, strain relaxation contributes to the junction quality by minimising the formation and propagation of defects.

Fig. 3.2e, f shows the charge separation in axial/substrate and radial/embedded junctions. In theory, the radial design is superior to the axial in terms of carrier

collection, since it occurs in an orthogonal way reducing the recombination probability. This is further enhanced by the fact that carriers are required to travel shorter distances to be collected due to the ‘embedded’ depletion region, which surrounds the absorber. However, although the radial geometry can minimise recombination losses in the quasi-neutral region, according to Kayes¹¹⁴, traps in the depletion region can have a severe impact on the open circuit voltage. Finally, the formation of radial tandem nanowire devices can be more demanding due to stress accumulation with increasing nanowire diameter.

3.3.2 Advantages of nanowire over planar devices

One of the advantages of nanowire solar cells over bulk and thin films is the lowering of the manufacturing costs. This is primarily due to material savings and the potential to use lower grade starting materials and substrates. In this section, the major benefits related to the optical, electronic and crystal structure properties of nanowires are analysed.

3.3.2.1 Optical properties

Nanowire arrays have the potential to minimise both reflection and transmission losses in solar cell devices. One of the standard methods, to minimise reflection losses in thin film and bulk solar cells is the use of anti-reflection coatings¹²⁸. Reflection occurs due to differences in the refractive index between two media and, according to Snell’s law, it is wavelength and angle-dependent. Therefore, several anti-reflection layers or layers with graded refractive indices are required for a wide spectrum response. Nanostructures and, specifically, tapered nanowires and nanocones, however, can act as a graded refractive layer with improved anti-reflection performance^{4,111,129,130} using only a single layer. Moreover, reports^{131–133} on the optical properties of nanowire solar

cells suggest that their exceptional antireflection performance can be maintained up to very high incident light angles.

In addition to their anti-reflection properties, ordered and randomised nanowire arrays can, potentially, enhance absorption due to strong light scattering. Muskens *et al*¹³⁴ have demonstrated that the optical mean free path, i.e. the average distance between light scattering events, can be significantly reduced using GaP nanowires. It was, further, shown that randomly distributed nanowires are more efficient in light trapping than ordered nanowires. This can be explained by considering the effect of diameter-dependent resonant modes in nanowires^{135,136}. Finally, the optical cross-section in nanowires has been found to be greater than the geometrical cross-section^{116,135,137,138}, a fact that can result in strong enhancement of the optical properties of nanowires.

3.3.2.2 Carrier separation and collection

Nanowires offer additional ways for charge separation, not available in planar films. Charge separation in nanowires can be enhanced due to quantum confinement effects in tapered structures. Specifically, the degree of quantum confinement depends on the nanowire diameter, which varies axially in tapered nanowires. Using density functional theory, it was shown¹³⁹ that this graded quantum confinement effect can result in successful separation of the charge carriers. In addition to this, theoretical calculations^{140,141} showed enhanced carrier separation nanowires. Further investigations, however, are required in order to implement them successfully in PV applications and benefit from lower recombination losses.

In addition to ‘exotic’ ways for efficient charge separation, nanowire radial junctions can offer enhanced carrier collection, since the diffusion lengths that carriers need to travel are shorter. Therefore, carrier collection in materials with low carrier diffusion

lengths can be improved. Indeed, theoretical calculations¹¹⁴ have shown that the Si nanowire solar cells can benefit from significant efficiency gains due to enhanced carrier collection. Enhanced carrier collection in solar cells comprising partly embedded CdS nanowires in a CdTe thin film has been experimentally and theoretically demonstrated by Fan *et al*¹²². In addition to this, lower resistive losses in single-crystalline nanowires are expected due to absence of grain boundaries, which can act as carrier scattering centres, carrier traps due to impurities or dangling bonds.

3.3.2.3 Strain relaxation

The maximum degree of mismatch that can be accommodated in nanowires without the formation of dislocations has been studied thoroughly^{142–146} showing that nanowires can relieve interface strain more effectively than thin films due to coherent expansion along the wire diameter.. The findings show that both in axial and radial heterostructures, a critical radius value exists, below which dislocations do not occur, independently of nanowire length. In nanowires with diameters that exceed the critical radius value, however, dislocations can occur for lengths that exceed a critical length value. Although most of the results suggest that effective stress relaxation occurs in relatively thin nanowires with diameters below 100 nm, there is no evidence that strain relaxation does not occur in thicker nanowires.

3.3.2.4 Exceeding the Shockley-Queisser limit

Nanowire solar cells have the potential to overcome¹⁴⁷ the predicted maximum efficiencies of the S-Q limit for planar devices due to reduced entropy losses^{148,149}. Moreover, even higher power conversion efficiencies can be achieved using tandem nanowire solar cells. Tandem nanowire cells can be developed using two main device configurations: a) a pure nanowire tandem structure, where multiple *p-n* junctions are stacked on top of each other and b) a hybrid planar-nanowire tandem structure, where a

nanowire p - n junction is developed on top of a planar p - n junction. Both architectures benefit from the strain relaxation and the enhanced optical properties of nanowires over thin films. Furthermore, the nanowire geometry enables an alternative route to current-matching in tandem cells by adjusting the NW geometrical properties, such as NW diameter, length or pitch^{150,151} instead of the layer thickness as in planar tandem devices. An example utilising the second device configuration is the nanowire-on-Si technology, which offers the potential of efficient and low-cost multijunction devices combined with the advantages of the Si solar cell industry. Many authors have investigated this architecture theoretically^{150–154}, while Yao *et al*²² have demonstrated a GaAs nanowire-on-Si tandem solar cell with efficiencies of up to 11.4%.

3.3.3 Challenges in the development of nanowire devices

3.3.3.1 Nanowire growth optimisation and junction formation

Here complications related to the growth of nanowires and the development of nanowire junctions are discussed.

Metal-catalysed nanowire VLS growth has been thoroughly investigated for many nanowire-catalyst material combinations and deposition techniques. However, since the growth regime for successful nanowire growth is relatively narrow, choosing the right conditions is not a straightforward procedure. The catalyst requirements (Section 3.2.2.2), the complexity of the phase diagrams, especially, in binary or even ternary systems and the characteristics and limitations of the various deposition techniques makes it difficult to predict and interpret the growth of nanowires. Furthermore, fine tuning of the growth conditions are required in order to control axial and lateral nanowire growth, which in some cases^{155,156} may be impossible.

A second nanowire-related complication is kinking, which occurs due to instability phenomena during growth^{157,158}. In catalysed VLS growth, the interface energies between the semiconductor materials and the catalyst alloy may cause the formation of kinked nanowires¹⁵⁹ in a similar way to Frank-van der Merwe¹⁶⁰ and Volmer-Weber¹⁶¹ growth modes. When the precipitated material from the catalyst forms a layer, straight nanowires are grown, while when it forms an island, kinked nanowires are grown. Usually, kinked nanowires are unfavourable in solar cell applications due to difficulties in the development of radial and axial tandem junctions, undesired crystallographic growth directions or defects that can hinder carrier transport.

An inherent complication of metal-catalysed nanowire growth is the ‘reservoir’ effect (Section 3.2.2.2), control over which is very crucial in the development of abrupt axial heterostructures^{162,163}. One approach to minimise the ‘reservoir’ effect is the use of catalysts with low solubility of the semiconductor material¹⁶⁴. Alternatively, Perea *et al*¹⁶⁵ have shown that the Si-Ge nanowire interfacial width can be systematically controlled by tailoring the Au-Ga catalyst composition, which, in turn, affects the semiconductor solubility in the catalyst. Wen *et al*¹⁶⁶ demonstrated the growth of atomically sharp Si-Ge interfaces using Al-Au catalysts, which remained solid during growth minimising the Si and Ge solubility.

Finally, formation of core-shell junctions can be challenging in randomly oriented nanowire arrays. This is because of shadowing effects during the vapour-solid deposition of the shell layer, which can result in non-uniform shell thicknesses or even discontinuities in the shell layer. Such phenomena can cause uneven stress in the nanowires affecting the mechanical and electronic properties and leakage currents, which can significantly impact the PV performance.

3.3.3.2 Carrier surface scattering and recombination

Due to the large surface-to-volume ratio, nanowire devices are likely to suffer from enhanced recombination through surface states¹⁶⁷. Schmidt *et al*¹⁶⁸, taking into consideration the effect of interface trap level density on the effective charge carrier density for thin nanowires, has derived an expression for a critical radius beyond which nanowires become fully depleted. In particular, unpassivated Si/SiO₂ nanowires with diameters of less than 300 nm and doping levels in the 10¹⁷ cm⁻³ regime are likely to be completely depleted by the surface states. Furthermore, Ford *et al*¹⁶⁹ have shown that carrier mobility decreases with decreasing InAs nanowire diameters due to surface scattering effects. A series of experimental evidence^{170–172} has shown that such effects can be limited by employing surface passivation layers.

3.3.3.3 Nanowire doping

Nanowires, being thin and long, are not ideal structures for doping using standard methods, such as diffusion or ion implantation. Alternatively, *in situ* doping of nanowires is possible during the metal-assisted VLS growth process. However, as discussed in Section 3.2.2.2, vapour species can be incorporated in the nanowires either by diffusion into the catalysts (axial growth) or by direct deposition on the nanowire sidewalls (lateral growth). This makes the control over the doping process challenging and can cause non-uniformities in the doping profile across the nanowires. Perea¹⁷³ and Koren¹⁷⁴ have shown that the dopants concentration in catalyst-assisted VLS grown nanowires increases radially and becomes maximum at the nanowire surface. This effect is further enhanced in tapered nanowires, where the distribution of dopants scale with the degree of tapering. The findings of Xie *et al*¹⁷⁵ show that nanowires with high concentration of dopants at the surface behave differently than nanowires with more uniform doping profiles and that thick nanowires tend to have more uniform distribution

of dopants than thin nanowires. This can be detrimental on the PV performance of radial solar cells and specifically on the V_{OC} values, where high and balanced doping levels are required^{109,176,177}. Indeed, the highest reported^{178,179} V_{OC} and FF values of radial devices have been found lower than that of axial nanowire and planar devices. For more detailed information on the doping of nanowires, the reader is referred to the comprehensive review of Wallentin¹⁸⁰.

3.3.3.4 Impurities incorporation

Catalyst or impurities incorporation into the nanowires or on the nanowire surface during growth is of great interest. For example, many reports demonstrate the incorporation of Au catalyst atoms in the bulk^{181–183} or the surface^{59,184} of Si nanowires during the Au-catalysed VLS growth. However, Au is known to form deep levels¹⁸⁵ in Si and Ge, which can reduce minority carrier lifetime and hinder PV performance. In addition to this, the incorporation of Au atoms in InAs¹⁸², GaAs^{186,187} and CdTe³⁵ nanowires with detrimental effects on their carrier transport and optoelectronic properties has, also, been reported.

3.3.3.5 Nanowire characterisation

The characterisation of NW arrays can be, often, problematic due to difficulties in determining the contribution of other layers that are probed during the measurement. Thus, single-nanowire characterisation is very important in understanding the transport, doping, surface, and charge separation properties of the nanowires. However, unlike bulk or thin film samples, probing a single nanowire is not a straight-forward procedure and, often, the extracted values contain significant errors. Simulations carried out by Khanal and Wu¹⁸⁸ have shown significant errors in mobility calculations using the infinite cylinder on a plane model. Additionally, the detection of impurities with very

low concentrations, such as Au catalyst incorporation in Si nanowires can be challenging^{181–183}, but of great interest, because they may hinder PV performance.

3.4 Review on nanowire solar cell devices

3.4.1 State of the art nanowire PVs

The advantages of the radial heterostructures were, first, demonstrated in a theoretical study by Kayes¹⁸⁹ in 2005. Two years later, in 2007, the first proof-of-concept single Si nanowire solar cell was developed by Tian *et al*¹²¹ and had a power conversion efficiency of 3.4%. Since then, a lot of research has been put in the development of efficient nanowire solar cells with impressive performance improvements. As a result, a GaAs single nanowire radial junction solar cell with an efficiency of 40% was demonstrated by Krogstrup¹¹⁶ in 2012. The exceptional, beyond the Shockley-Queisser limit, performance was ascribed to the outstanding optical properties, which resulted in J_{SC} values of 180 mA/cm². This is the record-efficiency of single NW devices until today. Below, a review of the record devices based on NW arrays is given.

The highest efficiency multi-nanowire solar cell device¹⁹⁰ has been presented in 2016 and is based on tapered axial InP nanowires. The nanowires were fabricated in a top-down approach by dry-etching epitaxially grown *n* and *p*-type InP layers. A power conversion efficiency of 17.8% was achieved by employing nanoparticles at the nanowire tips, which enhanced the optical absorption of the cell. This resulted in a short-circuit current of 29.3 mA/cm², which is similar to that of the record planar InP devices¹⁹¹. High PV efficiencies have been achieved in GaAs NW solar cell devices as well. In 2015, a GaAs axial NW solar cell with a certified efficiency of 15.3% was demonstrated by Åberg *et al*¹⁹². The nanowires were grown on patterned GaAs substrates using the Au-catalysed VLS growth method by means of MOCVD. The

authors ascribed the high conversion efficiency to the conformal coating of the GaAs NWs with a high-quality passivation layer. This resulted in exceptionally high V_{oc} values of up to 923 mV, which are comparable to those of planar GaAs record devices^{193,194}.

A radial GaAs NW device was demonstrated by Mariani *et al*¹⁷⁹ in 2013 with a record efficiency of 7.43% (this is the highest reported for radial NW devices). The device was based on GaAs *p-i-n* core-multishell nanowires grown by selective area catalyst-free epitaxy, which were coated by epitaxially grown window layers. The authors have shown both experimentally and theoretically, that by passivating the nanowires the surface recombination can be reduced, which is required in order to achieve high PV efficiencies.

3.4.2 CdTe nanowire PVs

A thorough search of the relevant literature regarding CdTe-based NW solar cells showed three main heterostructure geometries: radial, embedded and substrate heterostructures.

The highest efficiency for radial geometries was achieved by Williams *et al*¹⁹⁵ in 2013 using a core-shell ITO/ZnO/CdS/CdTe nanowire device. Au-catalysed CdTe nanowires were grown on CdTe-coated Mo foils by means of CSS deposition and coated with ITO/ZnO/CdS triple shells using sputtering deposition. High NW densities of 10^7 - 10^8 cm⁻² were achieved by using the CdTe buffer layers deposited on the Mo foils. This enabled faster saturation of the Au catalysts and resulted in up to 100 times lower reflectance compared to equivalent planar films. However, the maximum performance efficiency was as low as 2.49%, limited by significantly low J_{sc} , FF and V_{oc} values. Although a ZnO shell layer was used to reduce shunting effects, shunting was

considered to be the main cause for the low PV performance. A similar device with the same configuration, but without the inclusion of ZnO layer was reported by the author¹⁹⁶ of this thesis, addressing the low PV performance to shunting phenomena as well. The reader is referred to Chapter 6 for further work in the development of CdTe NW solar cells based on Au-catalysed CdTe nanowires. Other reported radial geometry implementations employ hybrid n-CdTe/P3OT¹⁹⁷, ZnO/CdTe/CuSCN¹⁹⁸, ZnO/CdTe^{199,200}, ZnO/CdTe QDs^{198,201–203} nanostructures with low, however, PV performance.

A second type of CdTe-based NW solar cells uses embedded heterostructures, such as CdS or ZnO/CdS core-shell nanowires in CdTe films. An efficiency of $\sim 6\%$ was reported by Fan *et al*¹²² using CdS nanopillars embedded in a 1- μm thick CdTe film. Using experimental and theoretical investigations, the authors showed that increasing nanopillar lengths improves the carrier separation and collection, but also interface recombination. Thus, although such structures may be beneficial in devices with short minority carrier diffusion lengths, surface recombination may be a limiting factor in devices with longer diffusion lengths. Major *et al*²⁰⁴ achieved an efficiency of 3.49% using ZnO/CdS nanowires embedded in a CSS-grown CdTe film addressing the relatively low performance to increased intermixing between the CdTe and CdS layers and shunting phenomena. An alternative approach was demonstrated by Dang *et al*²⁰⁵. CdS nanotubes were developed using electrochemical deposition and the inter and intra-tube space was filled with CdTe by means of CSS deposition. A well-defined junction was formed at the interfaces and due to the enhanced carrier generation, separation and collection properties, $J_{SC} = 25.5 \text{ mA/cm}^2$, $V_{OC} = 750 \text{ mV}$, $\eta = 10.7\%$ were achieved. Zhang *et al*²⁰⁶ have reported the development of a prototype core-shell nanostructured solar cell with a p - n CdTe-TiO₂ radial junction. This was accomplished by filling a

TiO₂ nanotube array with CdTe using pulsed laser deposition. However, only a very low estimated efficiency of ~ 0.1% was achieved. In this work, a maximum efficiency of 6.18% (Chapter 7) was achieved using ZnO/CdS core-shell structures embedded in a CdTe film.

Finally, devices with CdS nanowire/CdTe thin film substrate junctions have been implemented for solar cell applications. Dang *et al*²⁰⁷ have reported a power conversion efficiency of 11% using a nanowire CdS/CdTe thin film solar cell device. According to the authors, replacing the planar with the nanowire CdS layer enabled higher optical transmission in the CdS window layer and, thus, lower losses. This was confirmed by EQE measurements, demonstrating a relatively strong and wide spectral response. A similar configuration, i.e. a CdTe thin film device with a CdS nanowire window layer, but with lower conversion efficiency of up to 6.5% was demonstrated by Liu *et al*²⁰⁸. Major *et al*²⁰⁹ demonstrated CdTe/CdS thin film devices grown on a buffer layer of ZnO nanowires and the PV efficiency was evaluated for different nanowire lengths, i.e. 0, 0.25, 0.5, 1 and 2 μm . A maximum efficiency of 9.99% was achieved for zero nanowire lengths, i.e. planar ZnO film, while increasing nanowire lengths resulted in a gradual performance decrease. The main shortfalls were the low FF and V_{OC} , which the authors ascribed to recombination phenomena in the nanowires or at the various interfaces.

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4 Experimental methods

4.1 Introduction

This chapter describes the growth and characterisation experimental methods used in this thesis. It is divided in three main sections: In Section 4.2, the methods used for the deposition of thin-films and the growth of NWs are presented. Next, Section 4.3 describes the employed methods in order to obtain information for the structural, chemical and optical properties of the grown structures. Finally, Section 4.4 describes the methods used to characterise them and evaluate their performance.

4.2 Thin film and nanowire growth techniques

4.2.1 Close-space sublimation

The close-space sublimation is a simple and low-cost physical vapour deposition (PVD) technique and is widely used in the CdTe deposition of CdTe thin film solar cells¹⁻⁴. Some of the advantages over other CdTe thin film deposition techniques include the use of low-grade and cheap source material, high deposition rates and the potential for upscaling, which make it an ideal candidate for solar cell manufacturing. Additionally,

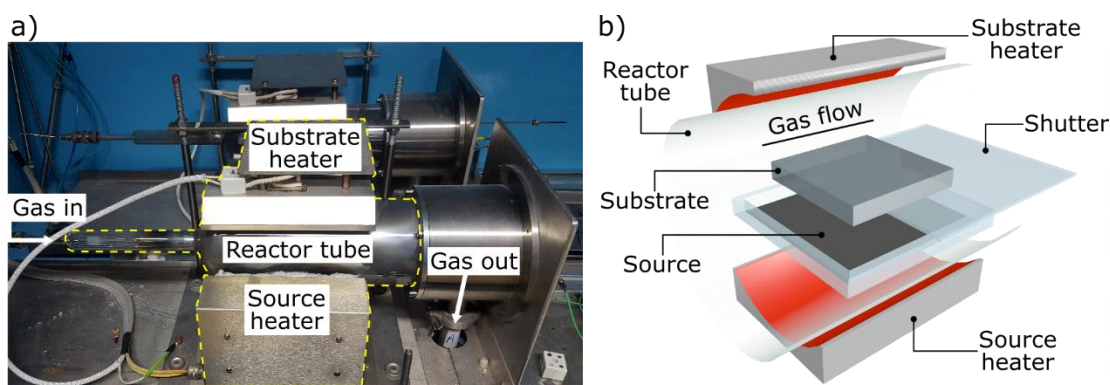
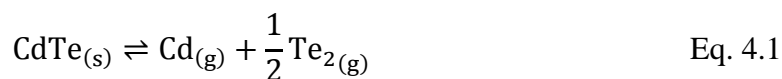


Fig. 4.1 Close space sublimation apparatus: a) Photograph of the Electro-Gas Systems Ltd. system and b) schematic diagram of the chamber.

due to the elevated substrate temperatures, CSS-grown CdTe polycrystalline films have grains several microns in size, these being considerably larger compared to other techniques (sputtered CdTe grain size is some tens of nanometres). Thus CdTe solar cells grown by means of CSS usually demonstrate higher power conversion efficiencies⁵.

CdTe CSS usually takes place between 500°C and 600°C and at pressures of some tens of Torr. Unlike to other techniques, this is achieved by placing the substrate in close proximity to the CdTe source (usually some millimetres or less). Under these conditions, the CdTe vapour pressure is sufficiently high (~ 0.001-0.027 Torr at 500-600°C) allowing the direct sublimation of CdTe and the dissociation to gaseous species:



Subsequently, the Cd and Te adatoms are transferred to the substrate due to the temperature gradient between the source and the substrate (usually < 100°C) and recombine.

Fig 4.1 shows the CSS system custom built by Electro-Gas Systems Ltd. used in the lab. The reactor's chamber, source tray and substrate holder are made of high purity

quartz in order to limit contamination from impurities. The CdTe source material used in this work (Alfa Aesar, 5N purity) was in the form of polycrystalline pieces (< 6 mm diameter) and polycrystalline fine powder depending on the experiment. The form of the source material affected the deposition rate⁶. The source, T_{src} , and substrate, T_{sub} , temperatures were controlled by two coiled heating elements, placed above and beneath the chamber and monitored by thermocouples. Although the heaters can be controlled independently, the source tray and substrate are thermally coupled, due to the very short distance between them. The temperature difference ranged from 40°C to 80°C. At the end of a run, the heaters can be slid away from the chamber allowing for high cooling rates. The chamber can reach base pressures in the range of $\sim 10^{-1}$ Torr using a scroll pump with the working pressures being from 5 to 100 Torr usually. Furthermore, the reactor can be operated under static fill or under gas flow of N₂, O₂, H₂, or N₂/O₂ or N₂/H₂ mixtures up to 100 sccm. Finally, the deposition onset can be controlled by a sliding shutter in order to have more control over the layer thickness.

As with other growth techniques, variables such as spacing, source and the substrate temperatures, pressure and the type of ambient gas have a direct impact on the film growth and consequently on its properties. Therefore, information about the exact growth conditions of each experiment is included in the experimental section of each results chapter.

4.2.2 Magnetron sputtering

Magnetron sputtering⁷⁻¹⁰ is used for the deposition of films and coatings at both the laboratory and industrial scales. It can be used for a wide range of materials from dielectrics and metals to semiconductors with the resulting films being of high quality, homogeneity and purity. The process begins with the ionisation of an inert gas, usually

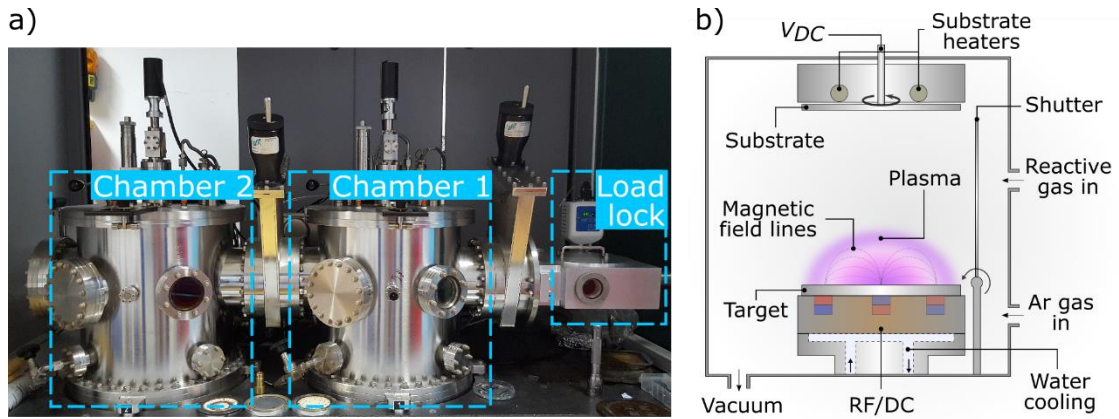


Fig. 4.2 a) Photograph of the dual Orion chamber system from AJA International Inc. b) Schematic diagram of the sputtering chamber.

argon, and the formation of the plasma. Depending on the type of the target material, a suitable high potential (DC for conducting materials and RF for insulating materials) is applied between the target and the substrate and the ions are accelerated towards the target. This bombardment causes the ejection of material from the target, which then condenses on all surfaces within the line of sight. In order to increase the deposition rates, magnets are introduced beneath the target. Upon collision of high-energy argon ions with the target, several species are ejected, such as neutrals, ions, X-rays, photons and secondary electrons. The ionisation and stability of the plasma can be greatly improved by confining the secondary electrons using a magnetic field. This results in higher plasma density in the vicinity of the target, which, in turn, enables higher deposition rates and lower operating pressures and voltages.

For the purposes of this work, three AJA International Inc. ATC Orion chambers were employed for the deposition of CdTe, CdS, SiO₂, Al₂O₃, Mo, Bi, ZnO and SnO₂:In films. These systems offer control over a series of variables such as, substrate temperature, T_{sub} , pressure, target – substrate spacing, RF/DC power, substrate bias V_{DC} , gas flow of N₂, O₂, H₂, or N₂/O₂ or N₂/H₂ mixtures. Moreover, each chamber contains more than one sputtering ‘gun’, which enables the fabrication of film stacks without

braking the vacuum or the simultaneous co-sputtering of different materials. For further details, the reader is referred to Refs.^{8,11}.

In a typical run, prior to the deposition of the material of choice, the chamber is pumped to a base pressure of 10^{-7} Torr. If needed, the substrate is heated to the desired temperature with the use of halogen lamps and, for uniformity reasons, the sample holder is rotated, since the magnetron ‘guns’ are not placed centrally. Next, 10-20 sccm of pure Ar or a mixture of Ar and H_2/O_2 is introduced and the pressure is set at 20 mTorr. The plasma is struck by ramping the DC/RF power to the target values. Finally, the working pressure is set to desired values (usually 2-10 mTorr) and the shutter is retracted from the line-of-sight between the target and the substrate. For a more detailed description of the growth parameters used in this work, the reader is referred to the corresponding experimental section of each chapter.

4.2.3 Thermal evaporation

Thermal evaporation or vacuum metallisation is one of the most common PVD techniques used for the deposition of metal, metal alloy or oxide thin films. The process involves the evaporation of the material of choice by means of a heating element (wire, basket, boat) or by electron beam bombardment inside a vacuum chamber. Since, usually, the material to be evaporated is located in the bottom of the chamber, the vapour rises and then condenses on the substrate, which is held face-down at the top of the chamber (Fig 4.3). The substrate temperature can be controlled via a resistive heating element and film homogeneity is improved by activating the substrate stage rotation. Typical pressures range from 10^{-5} Torr to 10^{-6} Torr. Finally, a shutter can be used to control the onset and completion of the film deposition.

For this work, 3 different thermal evaporation systems were used. Specifically:

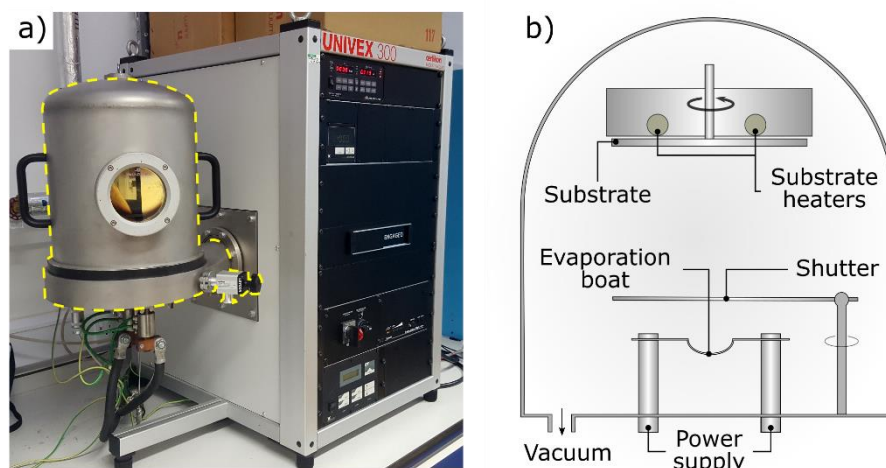


Fig. 4.3 a) Schematic diagram of a typical thermal evaporator chamber. b) Photograph of the Oerlikon UNIVEX 300 thermal evaporator used in the lab for the deposition of Au films

- Moorfield MiniLab 080 thermal evaporation system for the evaporation of Bi, Sb, Sn, Bi_2Te_3 , Zn, Cu
- Oerlikon UNIVEX 300 for the evaporation of Au and
- Moorfield M307 for the evaporation of Pt.

For this work, all thin film depositions were done with the substrate heater being turned off. Precise information about the evaporation of the above-mentioned films and their properties can be found in the experimental section of each chapter's results.

4.2.4 Spin coating

Spin coating is a simple and cheap widespread process usually used to deposit uniform coatings of organic materials¹² or to develop uniform distributions of particles¹³ on appropriate substrates. One advantage of this technique is its capacity to deliver very uniform films with thickness from few nanometres (or one monolayer in the case of particle distributions) to few microns in a couple of minutes. A typical spin coating process involves the casting of a solution of the desired material dispersed in an appropriate solvent, which is usually volatile, on a stationary or rotating (Fig 4.4). The rotation forces the solution to spread outwards and off, the edge of the substrate. The

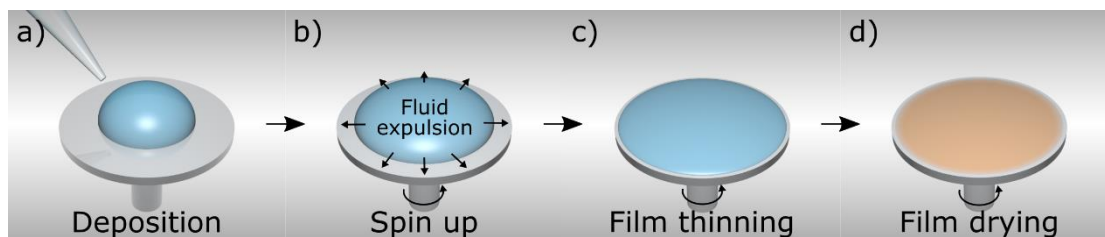


Fig. 4.4 Schematic diagram of a typical spin-coating process: a) First, a small amount of solution is dispensed on the substrate, b) the substrate is rotated at high speeds and the solution flows radially, c) thinning of the film occurs due to centrifugal acceleration and d) the solvent fully evaporates leaving behind the dried film

spin coating process may contain several spinning steps at different speeds and accelerations depending on the properties of the cast solution and the substrate (viscosity, drying rate, surface tensions, substrate roughness and hydrophilicity etc.). Finally, the deposited film is thinned down and dried due to the centrifugal acceleration along with the complete evaporation of the solvent. Typically, a conventional spin coater offers control over the spin speed, acceleration and time of each individual step of the process. More information about the spin coating process can be found in Refs. 14,15.

For the purposes of this work, a Laurell WS-650MZ-23NPP/UD2 spin coater was used to spin microsphere colloidal solutions on various substrates. These microsphere monolayers were used to form anti-dot templates in order to test the non-catalytic growth of CdTe nanowires. The reader is referred to Chapter 5 for detailed information about the spin coating process and the followed steps for the growth of the anti-dot templates and the CdTe NWs.

4.3 Thin film and nanowire characterisation techniques

This section describes the principles of the techniques used for structural, chemical, electrical and optical characterisation measurements.

4.3.1 Contact stylus profilometry

A surface profiler or profilometer is a common tool used to measure film step heights and film surface features, such as roughness and waviness. In a stylus profilometer, the probe (stylus) is moved along the surface of the sample and is in continuous contact. A force control system maintains a constant predefined force between the probe and the substrate and vertical displacements of the stylus are monitored by an optical deflection height measurement system. In this way, vertical resolutions that range from few tens of nanometres to millimetres can be achieved. In this work, an AMBIOS XP-Plus Stylus Profiler was used to measure the thickness of various films. The thickness was determined by measuring step height differences between the film's and substrate's surface. The steps were made either by masking the substrate during the deposition or by mechanical scribing or etching.

4.3.2 Scanning electron microscopy and microanalysis

A scanning electron microscope (SEM) rasters a focused electron probe over a sample's surface, generating a variety of signals – secondary and backscattered electrons, X-rays and visible photons – as products of the interaction between the high-energy electrons and the sample. These signals carry topographic, elemental and crystallographic information and can be recorded by appropriate detectors¹⁶. High magnifications (> 100,000×), large depth of field and remarkable picture clarity are some of the strengths of the SEM technique.

As shown in Fig. 4.5, a beam of electrons is generated by an electron source, such as a heated tungsten filament or a field emission gun. The electrons are accelerated towards the anode and a series of electromagnetic lenses is used in order to focus the beam on the sample. The focused beam is then raster scanned on the surface of the sample using

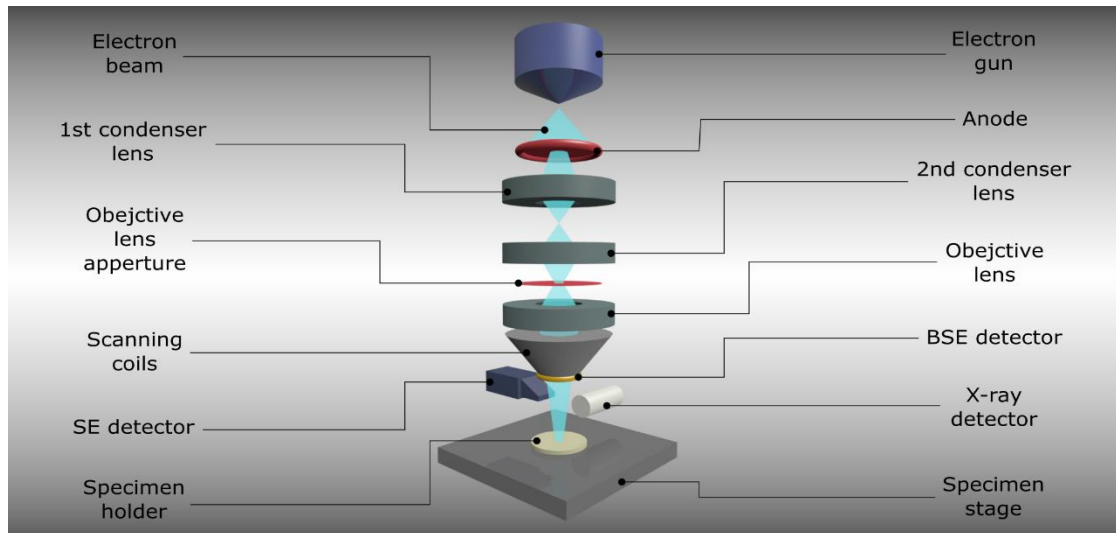


Fig. 4.5 Schematic diagram of a typical SEM column.

scanning coils. Secondary electrons (SE) are low-energy electrons generated by the ejection of electrons from the sample. Originating from surface, the SE are used for the acquisition of high quality topographical and morphological images. On the other hand, backscattered electrons (BSE) have higher kinetic energies than the SE and they are produced through elastic interactions of incident electrons with the nuclei in the specimen. Since atoms with higher atomic number cause stronger Coulombic scattering, the BSE images contain compositional contrast. Another phenomenon resulting from inelastic electron beam-specimen collisions is characteristic X-ray generation. Since the X-ray energies are characteristic of each element and the X-ray intensity increases with the element concentration, qualitative and quantitative elemental analysis can be performed.

Energy dispersive X-ray spectroscopy (EDS) systems are usually incorporated in both scanning and transmission electron microscopes allowing localised elemental analysis. One of the EDS analysis constraints is its spatial and depth resolution, which depends on the kinetic energy of the incident electrons and the mean atomic number, Z , of the sample. Fig. 4.6 shows the excitation volume: The higher the energy of the incident

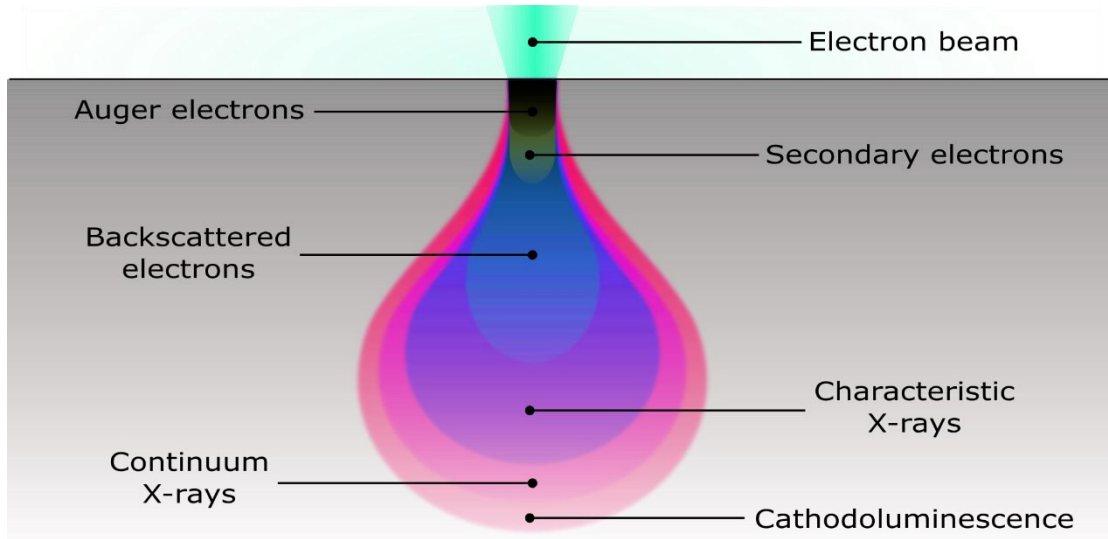


Fig. 4.6 Schematic illustration of the excitation volume caused by the electron-specimen interaction, demonstrating the generation depths of the various species.

beam, the greater the penetration and therefore the bigger, the excitation volume is. As a result the spatial and depth resolution of EDS/SEM analysis vary from some nanometres up to few microns¹⁶ and special care should be exercised when measuring structures with comparable dimensions, i.e. the nanowire structures studied in this work.

Finally, analysis of the electrical activity of semiconductors and semiconductor devices can be performed in an SEM microscope using the electron beam induced current (EBIC) technique. In this work, EBIC was used for imaging and characterisation of the *p-n* junction in solar cell devices. The working principle of this method is shown in the schematic diagram of Fig 4.7. The SEM electron beam rasters the sample's surface creating electron-hole pairs. If the electron-hole pairs manage to successfully diffuse to the depletion region, they will separate due to the electric field and a current will flow in the external circuit. The electron beam induced current is amplified and measured. By superimposing the EBIC signal with SEM micrographs, the position of the *p-n* junction and depletion region or electrically inactive areas can be imaged with high spatial resolution.

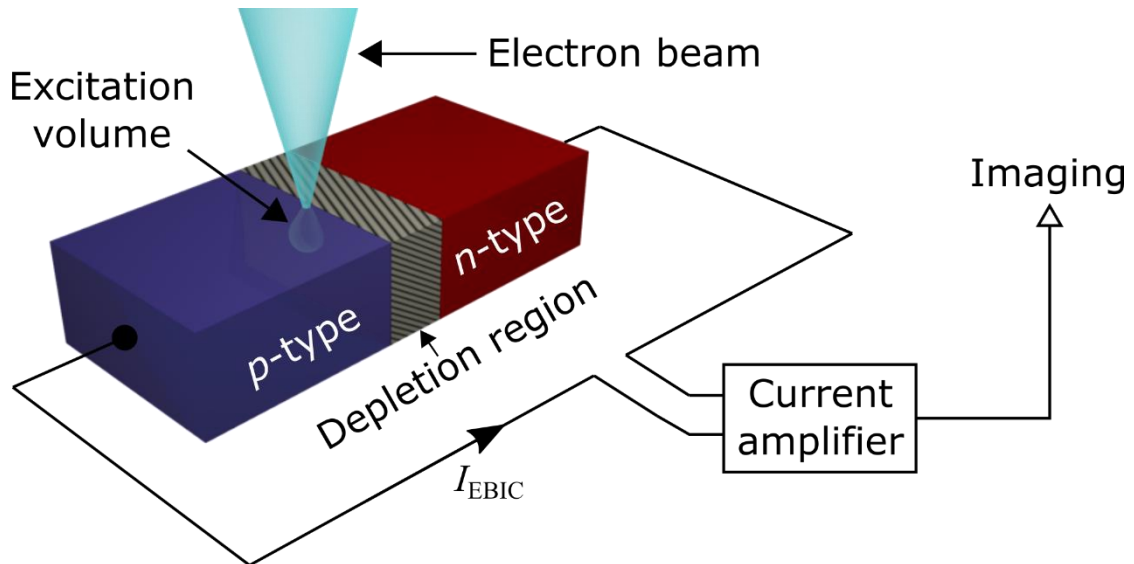


Fig. 4.7 EBIC schematic diagram.

In this work, all SEM/EDS measurements were carried on a Jeol JSM-7100F SEM in the nanoinvestigation centre at Liverpool. Topographical images and elemental analysis of thin films and nanostructures were acquired using mainly the SE, BSE and EDS modes. The reader is referred to Ref.^{16,17} for more information about other SEM characterisation modes and their application on thin-film solar cells. Additionally, thin films and nanostructures were modelled using the open-source software package, CASINO¹⁸ in order to estimate the origin of the EDS signal in these measurements. The software uses Monte Carlo algorithms to simulate the interaction of an electron beam with a bulk material and calculates the electron trajectories. EBIC measurements were performed by Mr L Bowen at the GJ Russell Electron Microscope Facility at Durham University on a Hitachi SU70 SEM with a Matelect ISM5 specimen current amplifier.

4.3.3 X-ray diffraction

X-ray diffraction (XRD) is widely used for the phase identification and structure characterisation of crystalline materials. The working principle¹⁹ of the technique is X-ray scattering and constructive or destructive interference, as described by Bragg's Law.

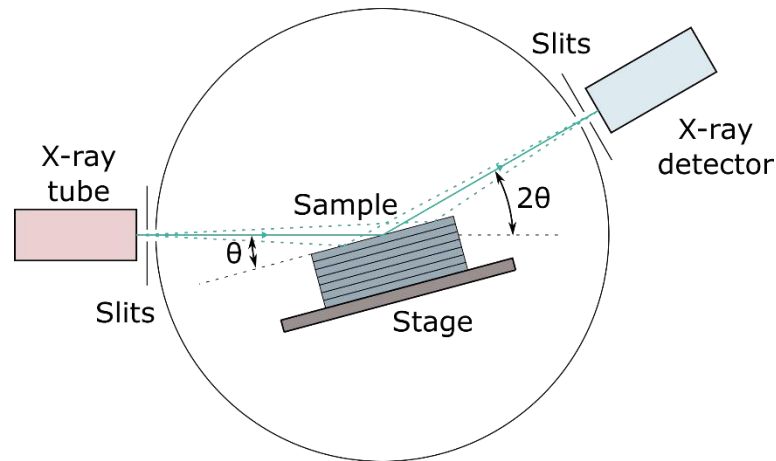


Fig. 4.8 Schematic diagram of a Bragg-Brentano diffractometer

which relates the X-ray wavelength to the angle of scattering from a lattice plane of spacing d_{hkl} by:

$$n\lambda = 2d_{hkl} \sin \theta, \quad \text{Eq. 4.2}$$

where n is a positive integer describing the order of diffraction, λ is the wavelength of the impinging electromagnetic radiation and θ is the incident angle. In the case of constructive interference, Bragg's Law is satisfied and the intensity of the diffracted x-rays is maximised.

The most common geometry of XRD setups is the parafocusing or Bragg-Brentano diffractometer and is depicted in Fig 4.8. A monochromatic and divergent X-ray beam, generated by a cathode X-ray tube, is directed to the specimen at an angle θ . Slits placed after the beam source (and before the x-ray detector) can be used in order to control the beam's angle of divergence. The X-ray beam is then diffracted by the sample and 'focused' to a detector at an angle 2θ . In this way, the sample's $\theta - 2\theta$ diffraction pattern can be formed by plotting the intensity of the diffracted beam against the angle 2θ . Since the incoming beam has a fixed, predefined wavelength, diffraction intensity peaks from certain hkl planes appear at certain 2θ angles according to Bragg's Law. In this way, the

respective characteristic d_{hkl} values can be calculated and compared to reference tables in order to acquire ‘fingerprint’ identification of the materials and crystallographic phases contained in the specimen. Moreover, for cubic materials the lattice parameter α can be extracted using the following formula:

$$\alpha^2 = (h^2 + k^2 + l^2)d_{hkl}^2 \quad \text{Eq. 4.3}$$

In polycrystalline materials, the relative degree of preferred orientation among the crystal planes can be evaluated using the Harris method^{20–22} and the texture coefficient TC_{hkl} :

$$TC_{hkl} = \frac{\frac{I_{hkl}}{I'_{hkl}}}{\frac{1}{n_p} \sum_1^{n_p} \frac{I_{hkl}}{I_{r,hkl}}} \quad \text{Eq. 4.4}$$

where I_{hkl} is the experimentally measured intensity of a given hkl -plane diffraction peak, I'_{hkl} is the standard intensity of the same peak of a randomly distributed sample taken from JCPDS reference tables and n_p is the number of peaks (or planes). The degree of preferred orientation in a thin film is deduced from the standard deviation, σ , of all the TC_{hkl} according to

$$\sigma = \left(\sum_1^{n_p} \frac{1}{n_p} (TC_{hkl} - 1)^2 \right)^{1/2} \quad \text{Eq. 4.5}$$

High σ values indicate stronger degree of preferred orientation. For the XRD characterisation performed in this work, a PANalytical X'Pert PRO MRD system was used.

The II-VI semiconductors may in principle adopt either the cubic zinc blende (sphalerite) or the hexagonal wurtzite lattices. These are most easily visualised with reference to the face centred cubic and close packed hexagonal lattices which are represented by the stacking sequences on the close packed planes ABCABC... etc and ABABAB... etc respectively. In the case of the binary II-VI semiconductors, there is a basis of one atom pair (e.g Cd-Te) at each lattice point. The two stacking sequences are therefore conventionally represented by Roman letters for the group II element and Greek for the group VI element and are $A\alpha B\beta C\gamma A\alpha B\beta C\gamma...$ etc (zinc blende) and $A\alpha B\beta A\alpha B\beta...$ etc (wurtzite)²³. Hence the two structures differ only in their second nearest neighbour interactions. The stabilisation of the zincblende over the wurtzite forms of the II-VI semiconductors has been calculated from first principles. CdS for example is stabilised in the wurtzite form by ~1 meV per atom and this accounts for its tendency to have a very high degree of stacking disorder in thin film form. CdTe on the other hand is stabilised in its zinc blende form by 6 meV per atom. This is an intermediate degree of stabilisation while there is little evidence for the existence of the wurtzite phase, the zinc blende material is nevertheless prone to planar defects, notably twinning. The two forms of the material may be distinguished by XRD studies which are expected to have systematic differences in the presence of lines and their intensities as shown in Table 4.1.

In practice while there are very many reports of XRD showing the zinc blende phase of CdTe there are very few that show the wurtzite phase^{24–26}. For the case of CdS, while the most stable phase is wurtzite, it is an over-simplification to say that samples comprise either wurtzite, zinc blende or some mixture of the two: Rietvelt analysis²⁷ has been used to demonstrate that CBD CdS films have XRD patterns that are not

Table 4.1 Structure factor calculations for zincblende and wurtzite CdTe

Zincblende		Wurtzite	
hkl	$ F ^2$	hkl	$ F ^2$
111	$16(f_{\text{Te}}^2 + f_{\text{Cd}}^2)$	10.0	$0.25(f_{\text{Te}} + f_{\text{Cd}})^2$
		00.2	$4(f_{\text{Te}}^2 + f_{\text{Cd}}^2)$
200	$16(f_{\text{Te}} - f_{\text{Cd}})^2$	10.1	$1.5(f_{\text{Te}} - 0.45f_{\text{Cd}})^2 + (1.67f_{\text{Cd}} - 0.866f_{\text{Te}})^2$
		10.2	$(0.5f_{\text{Te}} + 0.866f_{\text{Cd}})^2 + (0.866f_{\text{Te}} - 0.5f_{\text{Cd}})^2$
220	$16(f_{\text{Te}} + f_{\text{Cd}})^2$	11.0	$4(f_{\text{Te}} + f_{\text{Cd}})^2$
		10.3	$(1.5f_{\text{Te}} + 1.67f_{\text{Cd}})^2 + (0.45f_{\text{Cd}} - 0.866f_{\text{Te}})^2$
311	$16(f_{\text{Te}}^2 + f_{\text{Cd}}^2)$	11.2	$4(f_{\text{Te}}^2 + f_{\text{Cd}}^2)$
		20.1	$(1.5f_{\text{Te}} - 1.67f_{\text{Cd}})^2 + (0.866f_{\text{Te}} + 0.45f_{\text{Cd}})^2$
222	$16(f_{\text{Te}} - f_{\text{Cd}})^2$	00.4	$4(f_{\text{Te}} - f_{\text{Cd}})^2$

consistent with either pure phase, but arise from complex randomised stacking sequences.

4.3.4 Optical spectroscopy

Optical spectroscopy is a method used for transmittance and reflectance measurements of solids and liquids. In a spectrophotometer, a monochromated beam of light illuminates the sample and appropriate detectors measure the intensity of transmitted or reflected light. For both transmission and reflectance measurements, T and R are defined as the ratios of the measured quantity to the incident intensity. Furthermore, the absorption coefficient, α , can be extracted experimentally²⁸ using

$$\alpha = \frac{1}{d} \ln \frac{1 - R^2}{T}, \quad \text{Eq. 4.6}$$

where d is the film thickness. Subsequently, the optical band-gap, E_g , can be calculated from the respective Tauc plot²⁹, $(\alpha h\nu)^2 - h\nu$, where $h\nu$ is the photon energy. Although Tauc plots were initially developed to determine the bandgap of amorphous semiconductors, they are often used in crystalline semiconductors as well. Ideally, such

plots depict a distinct linear regime, which is the optical absorption onset of the material and the interception with the x-axis yields E_g according to Tauc's relation^{30,31}:

$$\alpha h\nu = A(h\nu - E_G)^n, \quad \text{Eq. 4.7}$$

where A is a constant and n is an exponent determined by the type of electron transition and is related to the shape of the conduction and valence band edges. In the case of direct bandgap semiconductors where the density of states depends on the square root of energy, n is equal to $\frac{1}{2}$. In this work, a Shimadzu SolidSpec-3700 spectrophotometer was used to measure the transmittance, reflectance and diffuse reflectance of films, nanostructures and solar cell devices for wavelengths in the 300-1100 nm regime.

4.3.5 Spectroscopic ellipsometry

Spectroscopic ellipsometry or ellipsometry is a characterisation technique used to measure films' thicknesses with angstrom resolution and materials' optical constants. The sample under investigation, which can comprise more than one layer, is illuminated with polarised light and the reflected light is recorded. The amplitude ratio of initial and detected polarised light, Ψ , and the phase difference, Δ , induced by the sample-light interactions are described³² as

$$\frac{r_p}{r_s} = \tan(\Psi) e^{i\Delta}, \quad \text{Eq. 4.8}$$

where r_p and r_s are the p - and s -components of the reflection coefficient. In order to extract the film thicknesses and optical constants a computational model is established, considering the optical constants and thicknesses of the sample's layer stack. Next, a preliminary guess is applied and unknown optical constant and thickness parameters are varied, while Eq. 4.8 is solved using the Fresnel equations for r_p and r_s . The best match

between the model and the experiment is determined in a regressive fashion using an estimator, usually, the mean squared error. Thus, the unknown parameters are varied until the MSE is minimised.

Ellipsometry measurements were performed by Dr R Treharne at the electrical engineering & electronics department of University of Liverpool on a Woolam M-2000-UI variable angle ellipsometer. For further information, the reader is referred to Refs.^{32–}

³⁴.

4.3.6 Atomic force microscopy

The atomic force microscope (AFM) is a characterisation tool used to obtain surface topography images with vertical discriminations from a few microns to some angstroms. AFM belongs to the broader scanning probe microscopes family, which were introduced after the invention of the scanning tunnelling microscope³⁵. One advantage of the AFM over the imaging techniques is its ability to produce 2- and 3-dimensional topographic images with extremely high resolution. On the other hand, AFM has image size constraints, slow image acquisition and images can suffer from artefacts arising from the tip characteristics.

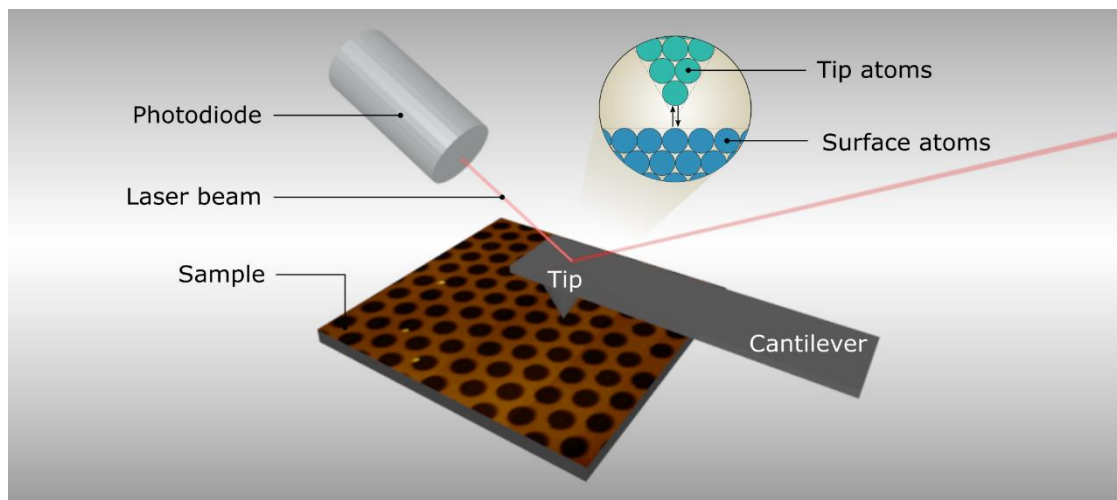


Fig. 4.9 Schematic illustration of atomic force microscope imaging principles.

The operation principle of the AFM and of all the probe microscopes is based on the interaction of the sample and a scanning probe³⁶ (tip). Specifically in an AFM setup, a nanometre sharp tip, mounted on a cantilever, raster scans the surface of the specimen either oscillating just above the surface or being in contact with the surface. Because of the sample's surface and the tip being close enough, various sorts of tip-sample interactions can appear. Typically, these interactions are van der Waals and coulombic forces, which deflect the cantilever towards or away from the surface. Cantilever deflections are monitored using an optical lever, which involves a laser beam reflected on the back of the cantilever and recorded by a position-sensitive photo diode, as shown in Fig 4.9. During an AFM measurement, the movement of the cantilever in X, Y and Z direction is controlled by a scanner, which is consisted of piezoelectric crystals. In this way, AFM images are obtained by recording the cantilever deflections when the tip passes over features on the sample's surface.

Surface characterisation and thickness measurements were performed by Dr. O S Hutter on a Veeco di Innova AFM and by Dr. Chu Li on a Bruker MultiMode 8 AFM at the University of Liverpool.

4.3.7 Raman spectroscopy

Raman spectroscopy is a light scattering measuring technique used for the qualitative and quantitative analysis of the molecular vibrations in a sample. A monochromatic laser source is used for the illumination of the sample and the scattered light is measured. Although almost all scattered photons have the same energy as the incident photons (Rayleigh scattering), a very small fraction of them can lose part of their energy due to inelastic collisions. Inelastic scattering occurs due to interactions of photons and the vibrating molecules and was first observed experimentally by Raman³⁷ in 1928. The

photon energy that is lost equals the energy of the vibrational mode of the scattering molecule. Thus, the recorded Raman spectrum, i.e. the plot of the intensity of the scattered photons against their frequency, can be used to identify the molecule or evaluate stress in the crystal structure. For more information the reader is referred to Ref.³⁸.

In this work, Raman spectroscopy measurements were performed in order to evaluate the effects of the MgCl_2 treatment on the crystal structure of CdTe thin films on a HORIBA XploRA PLUS Confocal Raman Microscope at the University of Liverpool. The microscope was equipped with a 532 nm laser (25 W maximum power output). The data points were collected using 5 secs acquisition time and 20 accumulations per spectrum with the rest of the acquisition settings being 2400 gr/mm grating, 200 μm slit, confocal hole of 500 μm and x100 objective lens magnification. 10, 25, 50 and 100% transmittance filters were used to modulate the laser beam power.

4.4 Solar cell performance characterisation

4.4.1 *J-V measurements*

The PV performance of thin film and NW solar cell devices was evaluated using current density-voltage measurements. The measurements were performed on a TS Space Systems solar simulator at room temperature under AM1.5 illumination spectrum with an intensity of 1000 W/m^2 . The calibration of the solar simulator was carried out using a GaAs reference cell. The *J-V* curves were obtained by sweeping an external voltage from the -1 to +1 V using a Keithley 2400 source meter unit and a LabView software interface was used in order to extract the key performance parameters, η , V_{OC} , J_{SC} and FF as well as R_S and R_{SH} .

4.4.2 *J-V-T measurements*

Temperature-dependent current density-voltage measurements were used to analyse the carrier transport limiting effects and calculate the back-contact barrier height of solar cell devices. The samples were placed in a Janis CCS-450 cryostat and *J-V* measurements were performed under dark conditions using a Keithley 2400 source meter unit and a LabView software interface in the -1 to +1 V range. A Lake Shore 331 system was used to control the temperature, which ranged from 250 to 300 K and increased in 5 K increments. The back-contact barrier height was determined using the method of Bätzner³⁹. According to this method, the total series resistance, R_S , can be expressed as:

$$R_S = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T} T + \frac{C_x}{T^2} e^{\Phi_B/kT}, \quad \text{Eq. 4.9}$$

where $R_{\Omega 0}$ is the Ohmic resistance, $\frac{\partial R_{\Omega 0}}{\partial T} T$ its temperature coefficient, $\frac{C_x}{T^2} e^{\Phi_B/kT}$ the thermionic emission component due to the flow of carriers over the back-contact barrier and C_x is a constant. The barrier height was determined by fitting the measured *J-V* extracted R_S values at different temperatures to Eq. 4.8. However, this method is valid only when the main and the back-contact depletion regions do not overlap.

4.4.3 *C-V measurements*

Capacitance-voltage profiling measurements were used to estimate the depletion region width, W , and the doping density, N , of solar cells. A p^+-n junction is assumed, where all the dopants are fully ionised and, therefore, the carrier concentration is equal to the dopant concentration. The depletion region can be considered as a capacitor sandwiched between the two semiconductors. Its capacitance is given by:

$$C = \frac{dQ}{dV} = \varepsilon \varepsilon_0 \frac{A}{W}, \quad \text{Eq. 4.10}$$

where A is the contact area. For the calculation of the doping density, an incremental voltage increase is assumed, which results in a charge increase given by:

$$dQ = qN_{(x)}dW \quad \text{Eq. 4.11}$$

Using Eq. 4.9 and 4.10, one can derive the following expression⁴⁰:

$$\frac{d(1/C^2)}{dV} = \frac{2}{\varepsilon \varepsilon_0 A q N_{(x)}} \quad \text{Eq. 4.12}$$

The left part of Eq. 4.10 can be calculated from the slope of $1/C^2$ versus V plot obtained from the C - V measurements. In this way, the doping density can be extracted. The C - V measurements in this work were performed in the dark using a Solatron SI1260 impedance analyser in the -1 to +1 V range and a frequency of 50 kHz.

4.4.4 EQE measurements

The external quantum efficiency (EQE) measurement is one of the most widely-used characterization tools in photovoltaics for quantifying the conversion efficiency of light electricity. It is defined as the ratio of the number of photogenerated charge carriers that are successfully collected by the solar cell to the number of illuminated photons at a certain wavelength. Ideally, the EQE becomes 100%, if all impinging photons with above band-gap energies are absorbed and the generated charge carriers are successfully collected. In reality, however, carrier recombination and optical losses act to reduce the quantum efficiency of solar cell devices. Fig.4.10 shows simulated *EQE* spectra of CdTe/CdS ‘superstrate’ solar cell devices on ITO-coated glass substrates using SCAPS. As discussed in 2.3.2.3, photons with energies higher than the CdS bandgap ($\lambda < \sim 512$

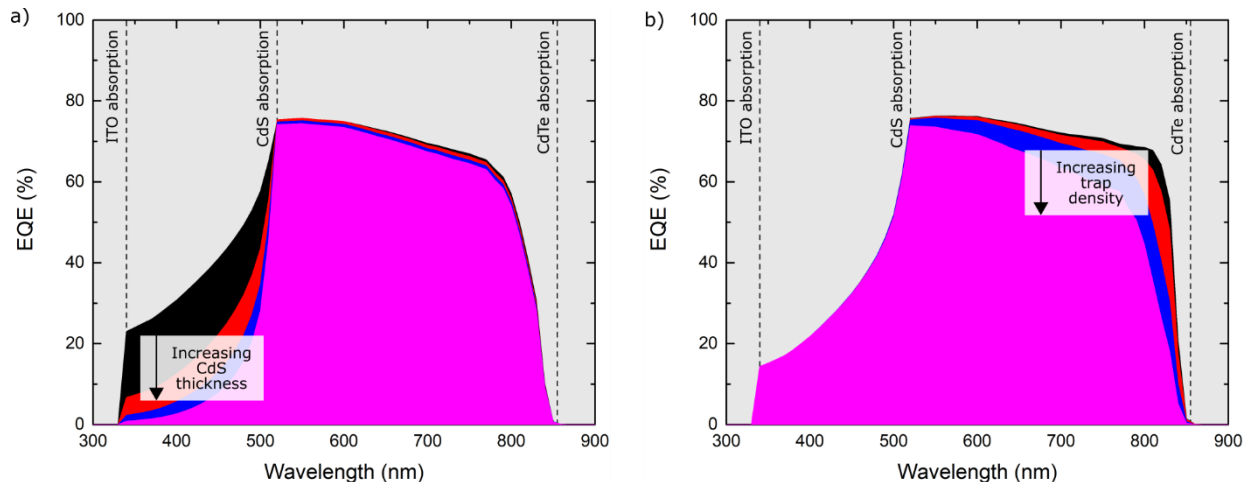


Fig. 4.10 Simulated EQE spectra (SCAPS) of CdTe/CdS devices demonstrating the effect of (a) parasitical absorption in the CdS window layer for increasing CdS layer thicknesses and (b) decreasing carrier lifetime in the CdTe absorber layer for increasing trap densities. The dashed vertical lines show the absorption edges of CdTe, CdS and ITO layers.

nm) are absorbed in the CdS layer, but do not contribute to the photocurrent due to enhanced carrier recombination and, therefore, significant *EQE* losses can be observed. One way to limit current losses due to parasitic absorption is to thin down the CdS layer (Fig. 4.10a), which enables higher transmittance of light. Fig 4.10b shows the impact of decreasing carrier lifetime in the CdTe layer on the *EQE* response; an increasing trap density in the absorber layer leads to decreasing carrier lifetimes and, hence, to higher *EQE* losses. The effect is more intense at longer wavelengths, since in this spectral range the *e-h* pairs are generated deeper in the device and need to diffuse for longer distances in order to reach the depletion region. Thus, higher losses due to non-radiative recombination are observed. Parasitical absorption in the ITO front contact (< 340 nm) or optical losses due to reflections at the front surface and at the various interfaces may lead to further *EQE* shortfalls. The reader is referred to the results sections of Chapters 6 and 7 for a comprehensive analysis of the EQE measurements of CdTe/CdS solar cells.

The spectral response of planar and NW solar cells was evaluated using a Bentham PVE300 system calibrated using a Si photodiode. The samples were illuminated in the 300 to 900 nm spectral range by a monochromatic light coming from a xenon lamp and a monochromator and the photogenerated current was amplified using a lock-in amplifier and recorded. The external quantum efficiency was obtained using the BenWin+ software.

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5 Growth studies of CdTe nanowires using template assisted and vapour-liquid-solid growth methods

5.1 Introduction

In this chapter, the growth of CdTe nanowires using the catalysed VLS growth method and a catalyst-free template assisted growth method is explored. Au is commonly used in the catalysed VLS growth of Si¹⁻³, GaAs^{4,5}, InAs⁶, InP⁷, ZnO⁸, CdS⁹ and CdTe¹⁰⁻¹² nanowires. However, CdTe/CdS core-shell nanowire PV devices incorporating Au-catalysed VLS grown CdTe nanowires demonstrated very low conversion efficiencies¹³. It was postulated that one performance limit in these devices was the Au forming deep level in the CdTe and reducing the quality of the PV junction. Therefore, the catalysed VLS growth of CdTe nanowires using both Au and alternative catalysts and the catalyst-free template assisted growth of CdTe nanowires were investigated. Following this, six different catalysts were tested for the catalysed VLS growth of CdTe nanowires and the catalyst-free selective-area epitaxial growth of CdTe nanowires using

two different template types was explored. While the template-assisted growth experiments did not yield any nanowire growth, the development of CdTe nanostructures by means of Au- and Bi-catalysed VLS methods was successful. However, due to reproducibility issues in the Bi-catalysed growth process, only the Au-catalysed CdTe nanowires were suitable for the development of CdTe/CdS core-shell nanowire PV devices which is presented in Chapter 6. For a detailed description of the catalyst-free selective area and catalyst-assisted VLS NW, the reader is referred to Section 3.2.2.

In Section 5.2, the fabrication and characterisation techniques and the experimental processes employed are described. In order to investigate the selective area epitaxial growth of CdTe nanowires, two different template types were explored: an ultra-thin dielectric film exhibiting a random distribution of pinholes (*holey* template) and a patterned antidot dielectric film (*antidot* template) developed using the nanosphere lithography technique¹⁴ (NSL). The hypothesis under investigation was that gaps in the oxide films may act as nucleation centres and result in the epitaxial growth of CdTe nanowires on the underlying CdTe buffer layer.

In Section 5.3, results on the development of the two templates used for the non-catalytic CdTe nanowire growth are presented. AFM, SEM and EDX measurements of SiO₂, Au and Mo antidot templates grown on bare and CdTe-coated glass substrates are presented in Section 5.3.2. Template assisted growth of CdTe nanowires using RF sputtering and sublimation (CSS) techniques is evaluated, but these methods proved to be less effective than VLS growth.

Next, results on the metal-catalysed VLS growth investigation of CdTe nanowires are presented. Section 5.4 describes the growth of Au-catalysed CdTe nanowires and

Section 5.5 the growth of Bi-catalysed CdTe nanowires. Bi_2Te_3 , Pt, Sb and Sn catalysts were evaluated but were less effective than Au and Bi (Appendix B).

5.2 Experimental

In this section, the experimental procedures and the growth conditions used for the templated and catalysed VLS CdTe nanowire growth investigations are presented together with details of the characterisation techniques used (the reader is referred to Chapter 4 for more background information on the growth and characterisation methods).

5.2.1 *Experimental procedures and growth conditions*

5.2.1.1 *Template-assisted growth investigation of CdTe nanowires*

Schematic diagrams of the two template-assisted NW growth processes under investigation are shown in Fig 5.1. In the top, a very thin oxide film is RF sputtered on a CdTe-coated substrate and due to the low surface coverage, the formation of a self-assembled random distribution of pinholes occurs. In this work, the formation of Al_2O_3 and SiO_2 holey templates was investigated by RF sputtering of thin-films on bare and CdTe-coated glass substrates and Si, GaAs and InAs wafers. In the nanosphere lithography approach (Fig 5.1b), monolayers of polystyrene (PS) spheres are spin-coated on a CdTe-coated substrate and, subsequently, their size is tailored by oxygen plasma etching. Next, thin films are deposited on top and the PS spheres are selectively etched away. In this work, the development of SiO_2 , Al_2O_3 , Mo and Au antidot templates was investigated by RF sputtering and thermal evaporation of thin films on bare and CdTe-coated glass substrates. In both cases, NW growth was tested using CdTe deposition by means of CSS and RF sputtering. The following is a description of the sample preparation steps and growth conditions used.

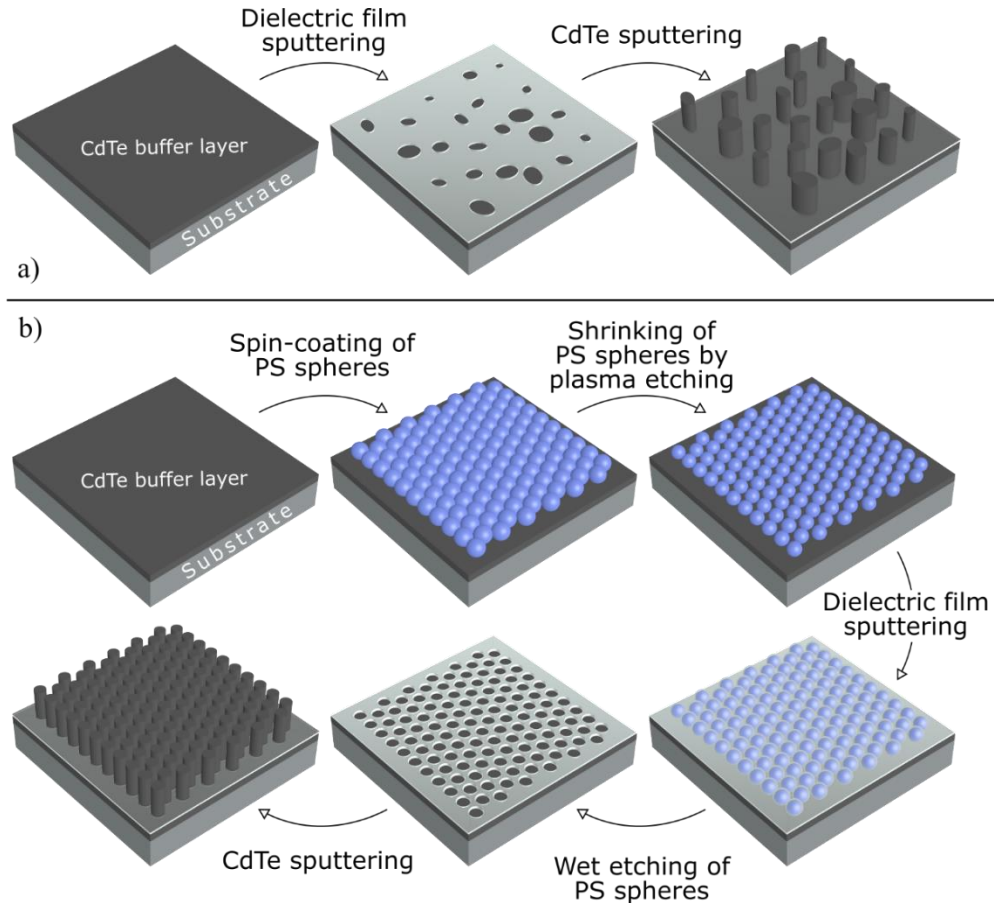


Fig. 5.1 Template assisted CdTe nanowire growth investigation: schematic showing the steps involved. Two different templates were tested: a) a thin dielectric film with self-assembled random pinholes and b) a patterned antidot dielectric film developed using nanosphere lithography with polystyrene (PS) spheres.

Substrate preparation: Pilkington Optiwhite 25 mm × 25 mm × 4 mm glass substrates and Si, InAs, GaAs wafers were ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N₂ gun. To remove all surface contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and dried with a N₂ gun again. Depending on the experiment, substrates were coated with Mo and/or CdTe layers. Mo buffer layers were RF sputtered using a 3'' × 0.25'' Mo target, 100 W power, 3 mTorr Ar pressure, 60 mins at 400°C (3.33 nm/min deposition rate). CdTe buffer layers were RF sputtered using a 3'' × 0.25'' CdTe target, 100 W power, 10 mTorr Ar pressure, 60 mins at 250°C (5 nm/min deposition rate).

Spin-coating of PS spheres: Commercially available 10% aqueous suspensions of PS spheres (Sigma Aldrich), 0.1 ($\sigma < 0.01 \mu\text{m}$), 1, 2 and 3 μm ($\sigma < 0.1 \mu\text{m}$) in diameter, were dispersed in ethanol (1:1 volume ratio). 50 – 80 μl of the aqueous ethanol solutions were spin-coated on bare and coated (Mo, CdTe) glass substrates. The spin-coating process comprised step a) rotation 500 rpm, acceleration 10 rpm/s, 20 secs, step b) rotation 2000 rpm, acceleration 1000 rpm/s, 2 mins and step c) rotation 4000 rpm, acceleration 1000 rpm/s, 20 secs. The solutions were dynamically cast onto the samples' surface during the first seconds of step a.

Radial etching of PS spheres in an oxygen plasma: Samples with spin-coated PS spheres were plasma etched in the AJA sputtering equipment at room temperature using 60 mTorr of oxygen pressure and a DC power of 10 W for times between 7 and 60 mins. The etching rate was 13 nm/min.

RF sputtering of SiO₂, Al₂O₃, Mo and thermal evaporation of Au thin films: SiO₂ layers were RF sputtered using a 3'' \times 0.25'' SiO₂ target, 100 – 300 W power, 2 mTorr Ar:O (0, 10% oxygen) pressure, 20 – 120 mins at room temperature (0.6 nm/min deposition rate). Al₂O₃ layers were RF sputtered using a 3'' \times 0.25'' Al₂O₃ target, 100 – 200 W power, 5 mTorr Ar:O (0, 10% oxygen) pressure, 60 – 120 mins at room temperature (0.17 nm/min deposition rate). Mo layers were RF sputtered using a 3'' \times 0.25'' Mo target, 100 W power, 3 mTorr Ar pressure, 15 mins at room temperature (3.5 nm/min deposition rate). Au layers were thermally evaporated to glass substrates with an evaporation rate of 1 Å/s.

Wet etching of PS spheres: Acetone, ethanol, toluene or CH₂Cl₂ were used for the removal of the PS spheres and the formation of the antidot template. The samples were

either immersed or ultrasonicated in beakers containing the etchant solutions. Finally, the samples were rinsed with DI water and dried with a N₂ gun.

CdTe NW growth investigation by means of CSS and RF sputtering: Samples with holey and antidot templates grown on coated (Mo, CdTe) and uncoated glass substrates were exposed to a CdTe flux inside the CSS and sputtering chambers. For the sputtering investigation, the conditions were 5 – 10 mTorr Ar pressure, substrate temperatures of 370°C, 400°C and 430°C, 60 – 100 W power, 2 – 20 mins deposition time. For the CSS investigation, a substrate temperature of 500°C and source temperature of 550°C were used under 10 Torr of N pressure for 5 mins.

5.2.1.2 Catalysed VLS growth investigation of CdTe nanowires

One of the requirements of the catalyst-assisted VLS growth of nanowires is that the catalyst should be in liquid form under the growth conditions. According to the Cd – Au, Te – Au and Cd – Bi, Te – Bi phase diagrams (Fig 5.3), all systems have liquid phases for temperatures < 500°C. Such substrate temperatures are accessible using CSS growth. The fabrication process of the catalysed VLS growth of CdTe nanowires is presented in Fig 5.2. Initially, thin catalyst films (Au, Bi, Bi₂Te₃, Pt, Sb, Sn) were deposited on bare or CdTe-coated substrates in an evaporator. The films were collapsed into spherically shaped catalyst particles by annealing and NW growth was achieved by exposure to a CdTe vapour flux. Both annealing and NW growth processes were carried out in a CSS chamber. The following is a description of the sample preparation steps and growth conditions used.

Substrate preparation: Pilkington Optiwhite glass substrates (4 mm thick), Si (111) and (100) wafers and Mo flexible foils (Advent Research Materials Ltd., 0.1 mm thick, 99.95% purity) were used. The samples were cut to 50 mm × 50 mm or 25 mm × 25

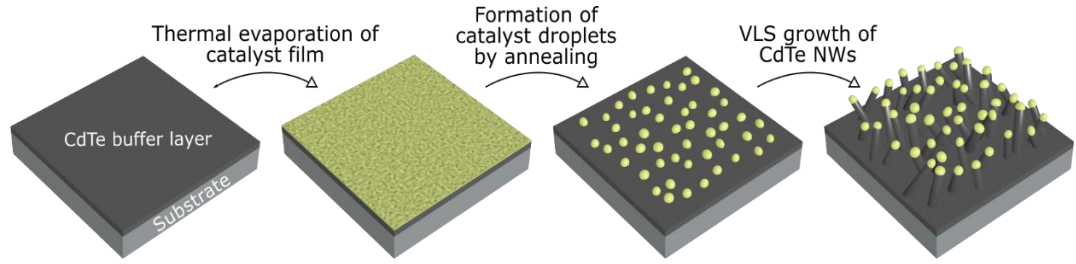


Fig. 5.2 Schematic of the catalysed VLS growth process of CdTe nanowires.

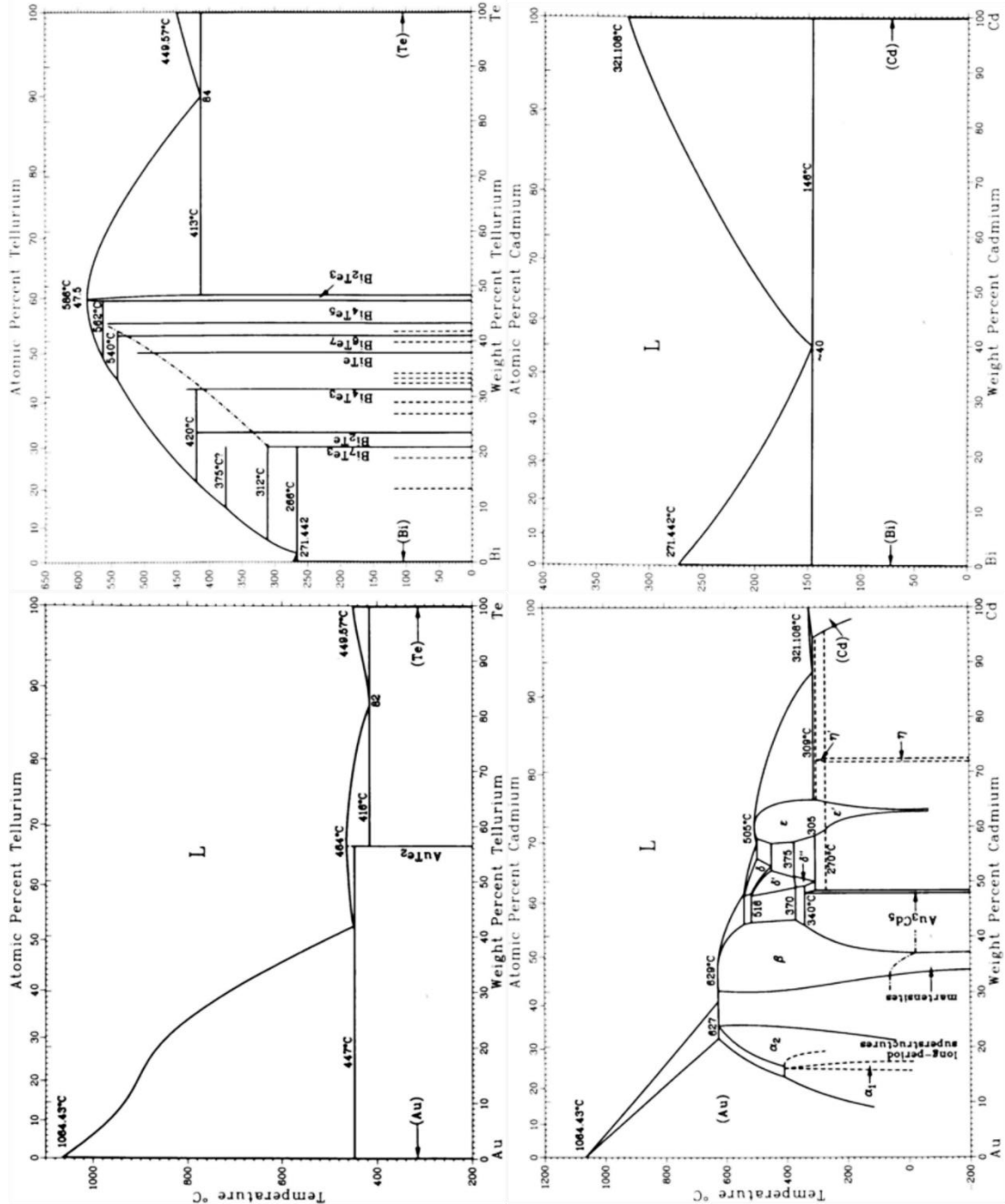


Fig. 5.3 Binary phase diagrams of Au – Cd⁵² (bottom-left) and Au – Te⁵³ (top-left), Bi – Te⁸³ (top-right) and Bi – Cd⁸² (bottom-right).

mm in size depending on the experimental procedure. Next, they were ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N₂ gun. To remove all surface contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and dried with a N₂ gun again.

Catalyst film deposition: Thin films of Au and Bi (5 – 20 nm) were thermally evaporated on bare and CdTe-coated glass substrates, Si wafers and Mo flexible foils. The thin film deposition was carried out at room temperature with a base pressure of $\sim 10^{-5}$ mbar and a growth rate of $< 1 \text{ \AA/s}$. A uniform film thickness across the samples area was achieved using a rotating sample stage.

Formation of catalyst droplets: Studies of the formation of catalyst droplets were carried out by annealing catalyst thin films deposited on Si wafers and bare and CdTe-coated glass substrates and Mo foils inside a box furnace and the CSS chamber. The conditions for the box furnace annealing experiments were 250 – 500°C in air for 0 – 60 minutes, while the conditions for the CSS chamber annealing experiments were 250 – 500°C, 5 – 300 Torr of static or dynamic H₂/N₂ ambient for 0 – 60 minutes. Both substrate and source heaters were used to achieve a uniform heat distribution. The average particles diameter and density was determined by using the ImageJ¹⁵ image analysis software and SEM micrographs.

CdTe NW growth investigation by means of CSS: Growth of CdTe NWs was achieved using Au and Bi catalyst nanodot arrays generated on Si wafers, CdTe-coated and bare glass substrates and Mo foils. The samples were exposed to a CdTe vapour flux inside the CSS chamber under controlled conditions; 460 – 570°C source temperature, 400 – 560°C substrate temperature, 5 – 40 Torr static or dynamic H₂/N₂ pressure, 0 – 90 minutes.

5.2.2 Sample sets

Overall, 85 samples were prepared for the templated growth investigation of CdTe nanowires (35 samples with holey templates and 50 samples with NSL generated antidot templates) and over 400 samples were fabricated for the catalysed VLS growth experiments. Further specific detail is included below to define differences between the sample sets. All samples were evaluated using AFM and SEM/EDX.

Development of holey templates: Although Al_2O_3 and SiO_2 thin-films (< 10 nm) were deposited on various substrates, no pinholes were detected on the dielectric films deposited on glass substrates and Si wafers. In Section 5.3, the SEM characterisation of 2, 5 and 10 nm thick SiO_2 films deposited GaAs wafers is presented.

Development of antidot templates: SiO_2 , Al_2O_3 , Mo and Au antidot films were developed on coated and bare glass substrates using the nanosphere lithography technique (Table 5.1). The spheres' initial diameter of 1 μm was reduced by 300 nm using O_2 plasma etching. Samples 'PS23' and 'PS27' were chosen to demonstrate the unsuccessful NW growth using SEM micrographs. The deposited CdTe layers had an effective thickness of 20 nm (sample 'PS23') and 80 nm (sample 'PS27').

Growth of CdTe nanowires using Au catalysts: The generation of Au nanodot arrays was investigated using samples with Au films (1.2 – 6.2 nm) deposited on Si wafers, Mo foils and CdTe-coated glass substrates. For the CdTe NW growth, the catalyst nanodot arrays and the CdTe NW growth processes were carried out inside the CSS chamber without braking the vacuum.

Growth of CdTe nanowires using Bi catalysts: Thin Bi films (1 – 10 nm) deposited on Si wafers, CdTe-coated and bare Mo foils. The Bi catalyst de-wetting and the NW

Table 5.1 Growth conditions of the samples used for the development of the antidot templates using colloidal masks. The reported thicknesses of the thin film layers are equivalent to films deposited on a glass substrate without the colloidal masks using the same conditions.

Sample	Buffer layers	Thin film layer
PS1	CdTe (300 nm)	SiO ₂ (40 nm)
PS12	CdTe (300 nm)	-
PS23	CdTe (300 nm)	SiO ₂ (80 nm)
PS27	CdTe (300 nm)	SiO ₂ (80 nm)
PS29	-	Mo (50 nm)
PS30	-	Au (40 nm)
PS36	Mo (200 nm)/CdTe (300 nm)	Mo (50 nm)
PS41	-	Al ₂ O ₃ (5 nm)

growth processes were carried out inside the CSS chamber without braking the vacuum.

For some experiments, the film annealing step was omitted.

5.3 Investigation of the template assisted, catalyst-free growth of CdTe nanowires

5.3.1 Development of holey templates

SEM morphological studies of Al₂O₃ and SiO₂ thin-films (< 10 nm) deposited on various substrates were difficult to interpret (Fig 5.4). In particular, the detection of pinholes on the surface of the dielectric films was problematic due to a combination of charging effects and low material contrast. Films deposited on Si wafers and glass

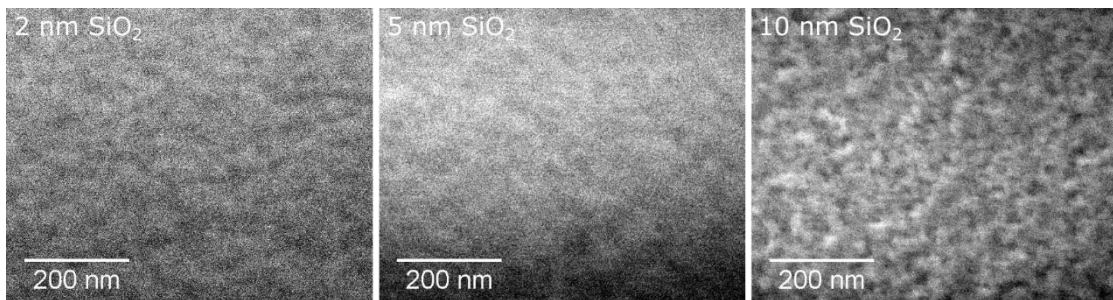


Fig. 5.4 Plan view SEM micrographs of 2, 5 and 10 nm thick SiO₂ layers deposited onto GaAs wafers.

substrates demonstrated no pinhole formation at all. Reducing the SEM's probe current and lowering the accelerating voltage diminished the charging effects, but also lowered the imaging resolution. Fig 5.4 demonstrates the surface morphology of 2, 5 and 10 nm thick SiO₂ films deposited on GaAs wafers: inhomogeneous contrast can be observed. Similar SiO₂ layers of same thicknesses were deposited on bare and CdTe-coated Si, GaAs wafers and glass substrates for use in the CdTe NW growth experiments. Overall, the formation of well-defined sputtered holey templates is uncertain and further investigation using other characterisation techniques, such as AFM is required.

5.3.2 Development of antidot templates

In this section, results on the spin-coating of polystyrene spheres and the generation of antidot templates on bare and CdTe-coated glass substrates are presented. Fig 5.5 demonstrates an incomplete monolayer of as-deposited PS spheres on a CdTe-coated glass substrate; short-range (tens of micrometres) close-packed sphere and disordered sphere arrays, sphere dislocations and sphere-free areas can be observed (areas with close-packed ordered domains aligned to different orientations forming domain

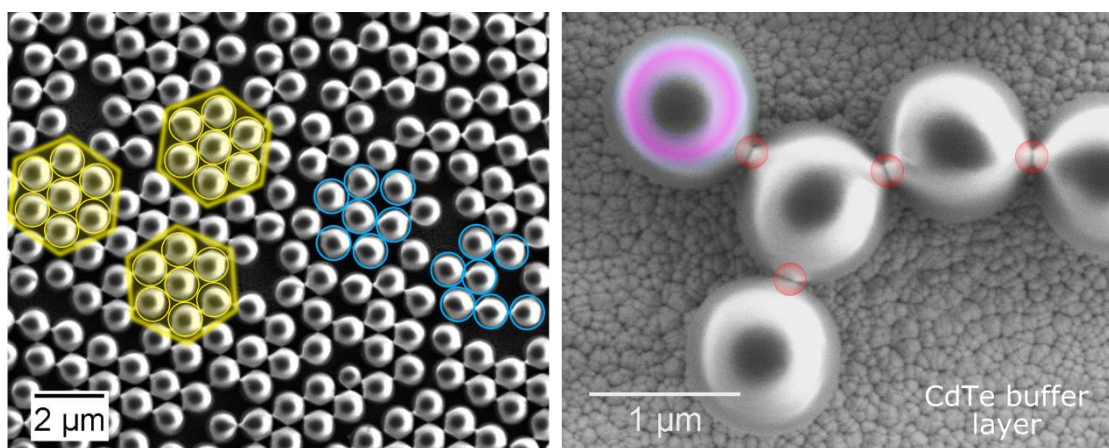


Fig. 5.5 SEM secondary electron micrographs of as-deposited PS spheres (1 μm) on CdTe-coated glass substrates; low (left) and high (right) magnification. Marked in yellow and blue are areas of ordered hexagonal close packed and disordered PS spheres. Right: the linking between the spheres (circled in red) and the glare effect (coloured in pink) are artefacts due to charging effects.

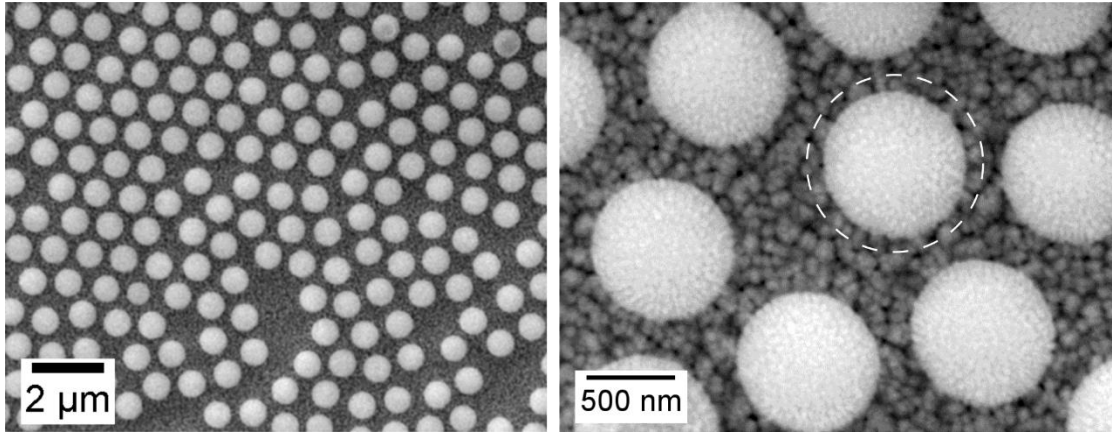


Fig. 5.6 Low (left) and high (right) magnification SE electron images of etched PS spheres deposited on CdTe-coated glass substrates. The spheres' initial diameter of 1 μm was reduced by 200 nm after a 15 mins plasma etching treatment. The roughness observed on the PS spheres is caused by the oxygen plasma etching.

boundaries and sphere multilayers were also identified, but not shown here). Next, oxygen plasma etching was used to reduce the spheres' size and separate them from each other (Fig 5.6). Thermally evaporated and sputtered thin-films were deposited on samples with arrays of radially etched spheres and, then, the spheres were removed. In Fig 5.7, the surface morphology of an Au antidot template generated on a glass substrate is demonstrated. The antidot array has an average thickness of 37 nm, hole size of 850 nm, hole pitch of 980 nm and a 45% surface coverage (5 nm thick Al_2O_3 templates with similar antidot arrays were also fabricated on glass substrates, but are not shown here).

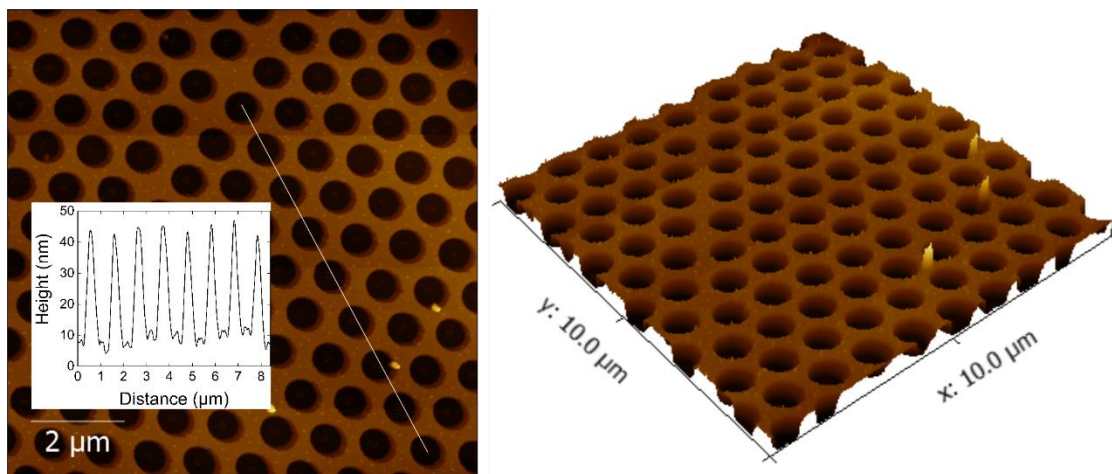


Fig. 5.7 2D (left) and 3D (right) AFM view of the surface morphology of an Au antidot film deposited on a glass substrate. Inset: height profile across the selected white line.

Molybdenum antidot templates fabricated on bare and CdTe-coated glass substrates are shown in Fig 5.8. In accordance with the Au, the Mo antidot arrays that were generated on uncoated glass substrates demonstrated close-packed ordered domains over large areas ($> 100 \mu\text{m}^2$). The average thickness was 50 nm, hole size 810 nm, hole pitch 1030 nm and surface coverage 46%. On the contrary, the sample with the CdTe-coated glass substrate demonstrated a disordered Mo hole array with an average thickness of 63 nm, hole size of 770 nm, hole pitch of 1030 nm and surface coverage of 17%. The average and *rms* values as well as the maximum height of the roughness were 7 nm, 9 nm and 44 nm respectively. In Fig 5.9, SEM and AFM surface micrographs of a SiO₂ template fabricated on a CdTe-coated glass substrate are shown. The average thickness was 43 nm, hole size 740 nm, hole pitch 990 nm and surface coverage 34%. The average and *rms* values and the maximum height of the roughness were 6 nm, 7 nm and 39 nm respectively. SEM/EDX measurements of the sample's surface from 5 different sites are presented in Table 5.2; spectra 'Sp.1', 'Sp.3' and 'Sp.4' were taken from points located in the holes, while 'Sp.2' and 'Sp.5' from points located in the SiO₂ film. As can be seen, the Si content measured at the holes is ~ 1 at.%, while that measured at the

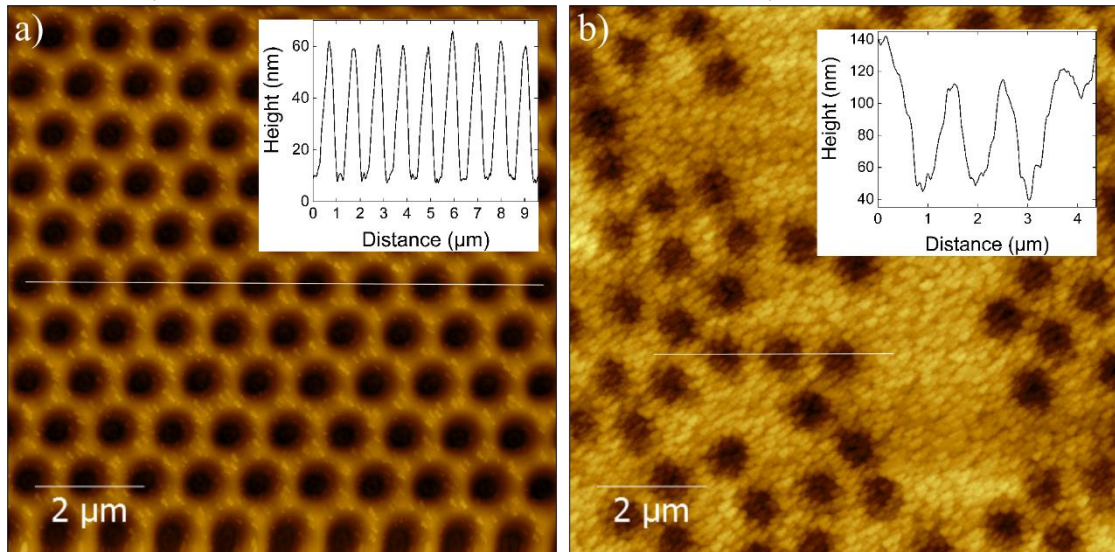


Fig. 5.8 2D AFM views of the surface morphology of Mo antidot films deposited on a bare (a) and a CdTe-coated (b) glass substrate. Insets: height profiles across the selected white lines.

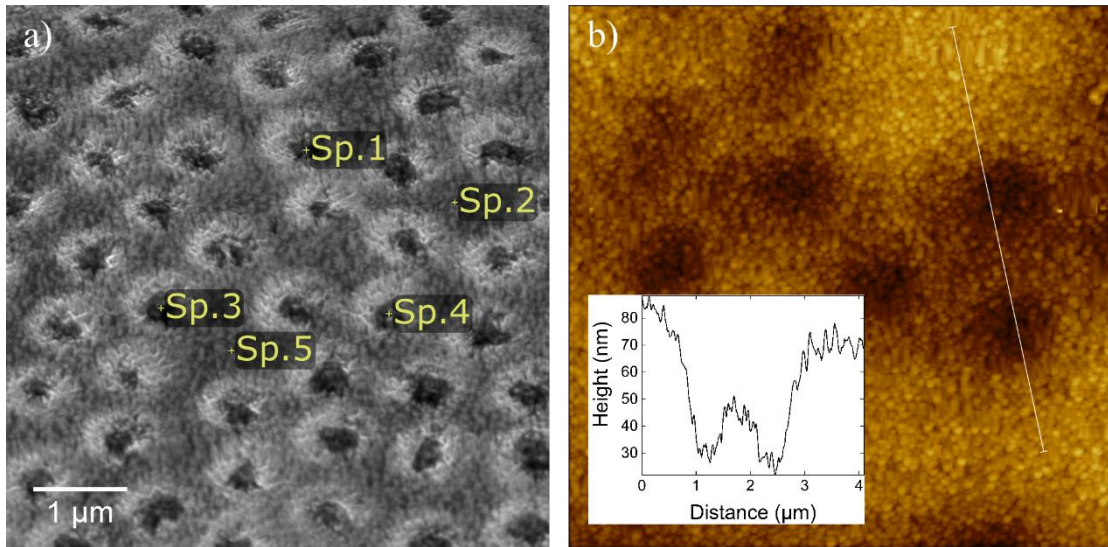


Fig. 5.9 a) 45° view SEM secondary electron and b) AFM micrographs of a SiO₂ antidot template fabricated on a CdTe-coated glass substrate.

Table 5.2 Surface SEM/EDX elemental analysis of the SiO₂ template shown in Fig 5.9.

Spectrum	O (at.%)	Si (at.%)	Cd (at.%)	Te (at.%)
Sp.1	8	1	47	44
Sp.2	41	8	26	25
Sp.3	5	1	48	46
Sp.4	8	1	46	45
Sp.5	39	9	27	25

continuous areas is 8 – 9%. Oxygen was detected in all 5 spectra with atomic concentrations of ~ 5 – 41%. These findings confirm the existence of a non-stoichiometric porous SiO_x film on the sample's surface. However, a quantitative determination of the film's stoichiometry is not possible due to contributions from oxides on the CdTe surface and the limited x-ray spatial resolution.

5.3.3 CdTe growth using holey and antidot templates

Although CdTe growth on both kinds of templates was attempted by means of CSS and sputtering using a wide range of conditions, SEM investigations revealed that it was not possible to fabricate nanowires. Variation of the template hole sizes in the range ~ 500 – 800 nm failed to encourage selective growth either in the windows or on the mask.

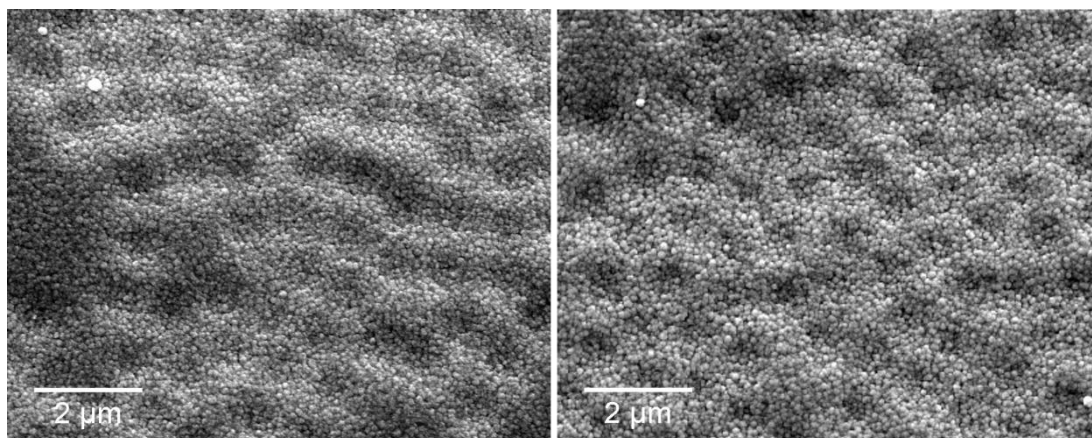


Fig. 5.10 SEM SE micrographs of representative samples with SiO₂ templates after 5 (left) and 20 (right) minutes of CdTe sputtering at 430°C (the deposited CdTe films have an effective thickness of 20 and 80 nm respectively). The SiO₂ antidot templates were generated on CdTe-coated glass substrates prepared using colloidal masks.

Instead, CdTe deposition occurred uniformly over both and the deposition was conformal with the underlying material. Fig 5.10 shows a typical example, this being for SiO₂ antidot templates on CdTe films. Sputtering of CdTe for 5 and 20 mins failed to give selective growth and the surface morphology represents that of the underlying material. Similar results were obtained for SiO₂/CdTe (PS1, 12, 23, 27), Mo and Au on glass (PS29, 30), Mo/CdTe (PS36) and Al₂O₃ on glass (PS41). Hence exhaustive tests failed to generate selective growth.

5.3.4 Discussion of the templated growth study of CdTe nanowires

5.3.4.1 Development of templates

The formation of sputtered holey templates (Section 5.3.1) could not be verified with certainty as described above and this made their use in templated growth uncertain.

On the contrary, the fabrication of a wide range of antidot templates using the nanosphere lithography technique was successful (Section 5.3.2). Al₂O₃, Au and Mo antidot arrays were generated on glass substrates with well-defined pores and large close-packed ordered domains. Attempts to form Mo and SiO₂ templates on CdTe-

coated substrates was less successful and generated pores with fuzzy boundaries. The characteristics of the deposited polystyrene sphere films, such as the degree of ordering and multilayer stacking, are strongly dependent on the spin coating parameters, the substrate wettability and the amount and properties of the colloidal solution¹⁶. Kralchevsky and Denkov¹⁷ have shown that capillary and hydrodynamic forces are the main driving forces that influence the ordering of spherical particles immersed in a wetting film on a horizontal substrate. Moreover, the substrate's properties (surface chemistry and roughness) can have a great impact on the wettability of the colloidal suspension and the substrate – sphere interactions. Although the surface roughness of the CdTe buffer layer is < 10 nm and comparable to that of the glass substrates, it is highly probable that the morphological differences of the generated templates is due to surface chemistry effects and differences in the sphere – substrate interactions. Therefore, a further optimisation of the spin-coating process is required for the CdTe-coated substrates in order to balance the sphere – sphere and sphere – substrate interactions and achieve a higher density of short-range ordered arrays.

5.3.4.2 Template-assisted CdTe nanowire growth investigations

The fabrication of CdTe nanowires using randomly distributed holey SiO₂ films was unsuccessful even though there is a literature report of it having being accomplished by Soshnikov^{18,19}. Although similar sample preparation procedures were used in this work, nanowire growth was not observed. It is likely that this was due to the incomplete formation of pores with the SiO₂ films in the present study, although as mentioned above the SEM images are inconclusive.

CdTe growth on antidot templates using a wide range of conditions (see 5.2.1.1) resulted in the conformal coating of the surface and no nanowire growth was observed. Template-assisted selective area nanowire growth starts with the preferential nucleation

of the adatoms in the pores. Most often nucleation commences at the pores' corners and the nucleation rate is strongly affected by the template's and underlying layer's surface properties and the pores' diameter and shape²⁰. In this way, the gaps in the antidot templates were expected to act as nucleation centres for the Cd and Te adatoms. AFM height profiles and SEM images showed that antidot templates fabricated on glass substrates (PS29, 30, 36 and 41) had pores with abrupt and well-defined sidewalls. This suggests that a high probability of nucleation and nanowire growth is expected for these samples. However, the absence of an underlying CdTe buffer layer (or any crystalline substrate), which would promote the homo- or hetero-epitaxial growth of CdTe may be a limiting factor. Although the mechanism behind the selective area growth of nanowires is still under discussion, studies of GaAs and InAs nanowires^{21–24} showed the epitaxial nanowire growth is a facet-dominated growth technique strongly influenced by the orientation of the substrate. Because of that, the growth of nanowires oriented along preferential growth axes at the template openings dominates over the lateral film growth. Although samples with SiO₂ antidot templates on CdTe (PS1, 12, 23 and 27) meet this requirement for epitaxial growth, selective nucleation and growth of CdTe crystals in the template openings was not observed. SEM and AFM investigations of antidot arrays on CdTe showed concave pores with fuzzy boundaries and gradual sidewalls. Moreover, SEM/EDX elemental analysis of sites located at the holes of SiO₂ antidot arrays formed on CdTe-coated glass substrates showed > 4 at.% O and < 1 at.% Si. On the contrary, in SEM/EDX measurements of CdTe back-surface of sputtered CdTe solar cells (Section 7.4.1) no Si or O traces were detected. This is a strong indication of the existence of surface oxides on the underlying CdTe layer, which may limit the selective nucleation of CdTe. Finally, the pores' diameter and pitch have been reported to influence strongly the nanowire growth rate or even shift the growth

of nanowires to that of large crystallites for increasing pore diameters^{25–27}. However, in this work the formation of distinct crystallites or nanowires at hole sites was not observed and therefore these factors can be ruled out. Thus, it is speculated that the pores' geometry or the oxidation of the underlying CdTe buffer layer during or after the formation of the antidot array are the reasons for the unselective conformal coating of the templates.

5.4 Growth of CdTe nanowires using Au catalysts

5.4.1 Development of Au nanodot arrays

Preliminary studies of the de-wetting of Au thin films on Si wafers and the generation of Au nanodot arrays are presented here. This gave considerable insight into the factors that influence the de-wetting process and the morphology of the nanodot arrays. Figures 5.11, 5.12 and 5.13 demonstrate the impact of the annealing time, Au layer thickness and annealing temperature on the nanodot characteristics. Plots of the average diameter and density of the nanodots for each case are shown in Fig 5.14. The three horizontal lines (top-to-bottom) of each box represent the 75th percentile, the mean and the 25th percentile values respectively. For each data bin, the individual data points are spread out horizontally in order to display all of the data without overlaps.

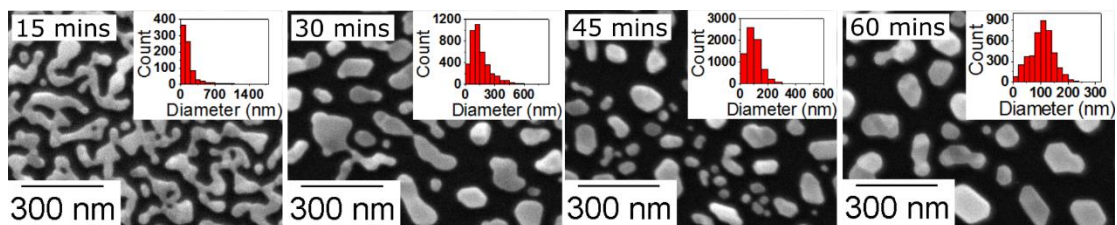


Fig. 5.11 Secondary electron SEM images of Au films (5.5 nm) on Si wafers. The films were annealed at 300°C in air for 15 – 60 mins. Initially, the film dewetting promotes the formation of small particles, which eventually coalesce into larger particles for longer annealing intervals. Insets: nanodot diameter histograms.

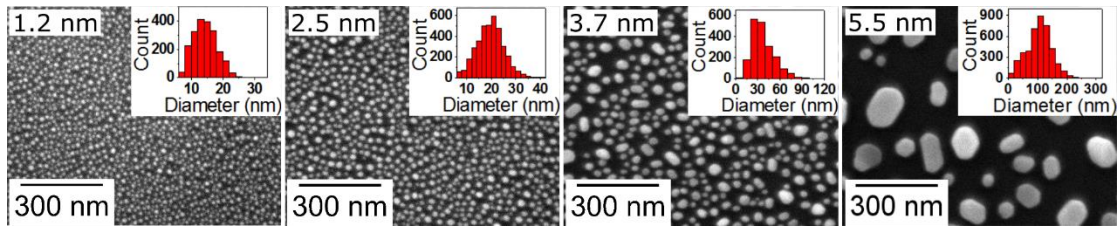


Fig. 5.12 Secondary electron SEM images of Au films with varying thickness (1.2 – 5.5 nm) on Si wafers. The films were annealed at 500°C in air for 30 mins. Increasing initial Au film thickness results in larger particles and lower surface coverage. Insets: nanodot diameter histograms.

SEM studies of the evolution of the Au film morphology with time revealed the following stages during annealing; firstly, the film collapsed into irregular stripes and small islands (15 mins). Subsequently, the irregular Au networks were broken into isolated particles (30 mins), which were further decomposed to smaller particles with increasing annealing times (45 mins). Eventually, for longer annealing periods (60 mins) the islands gradually coalesced into larger ones. A maximum nanodot density was observed after 45 minutes of annealing.

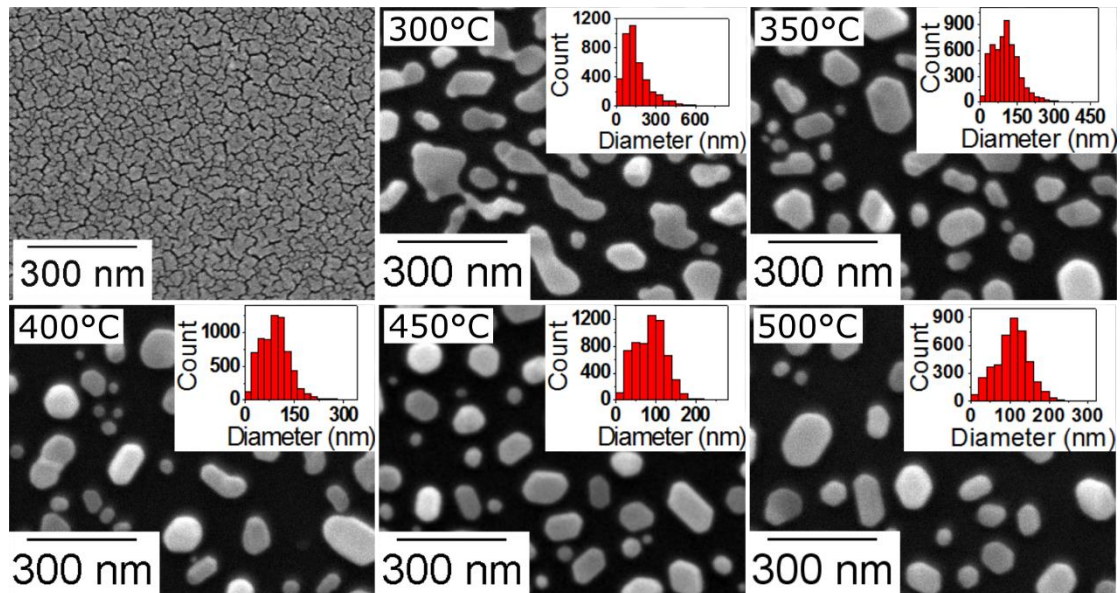


Fig. 5.13 Secondary electron SEM images of Au films (5.5 nm) on Si wafers. The films were annealed in air for 30 mins at 300 – 500°C. Increasing annealing temperatures promote the formation of small particles initially, which coalesce into larger particles at higher temperatures. Insets: nanodot diameter histograms.

Similar trends were observed for varying annealing temperatures at a given annealing period of 30 mins. For low annealing temperatures (300°C), the film disintegration into isolated islands was incomplete. At 350°C, isolated islands were observed, which decreased in size with increasing temperatures up to 450°C. Finally, at 500°C the particles' average size increased again. The width of the diameter distributions decreased inversely with annealing temperature. The nanodot density reached a maximum for the sample annealed at 400°C. Further increase in annealing temperature resulted in decrease in nanodot density.

SEM micrographs of annealed Au films (500°C in air for 30 mins) with varying thicknesses showed a monotonical exponential increase in average particle size with increasing initial film thickness. Moreover, a similar increase in the width of the diameter distributions was observed. The nanodot density decreased linearly with increasing film thickness.

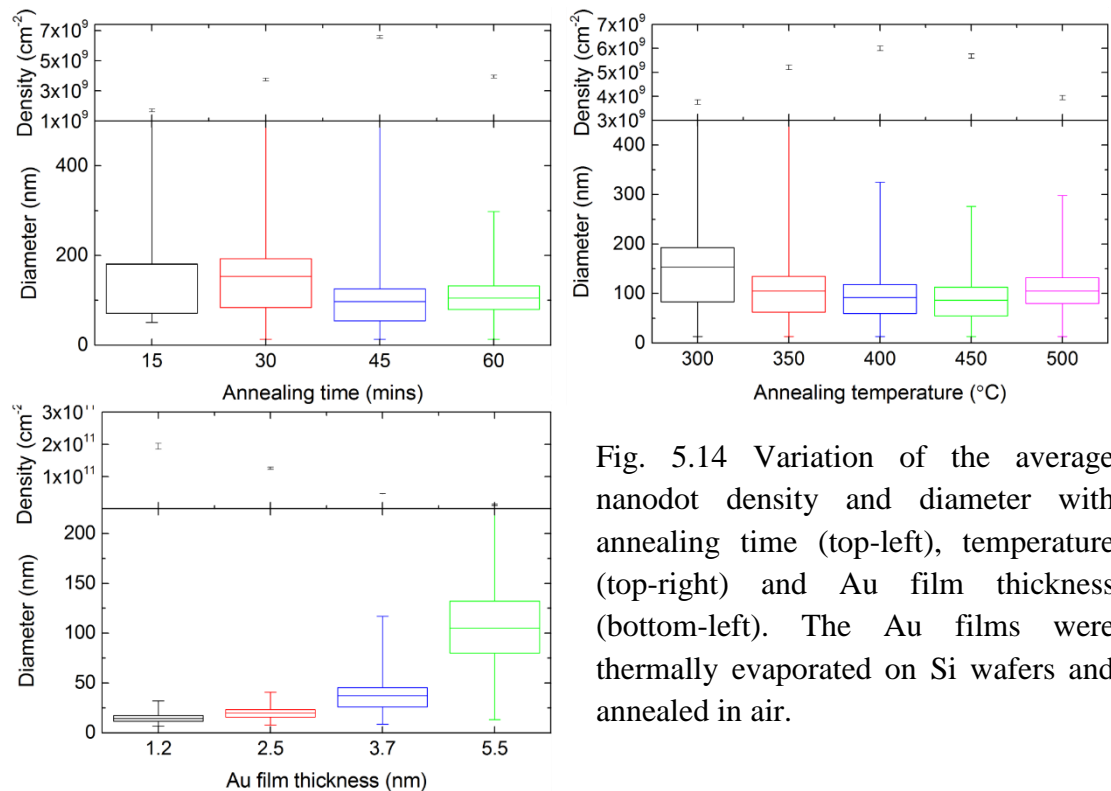


Fig. 5.14 Variation of the average nanodot density and diameter with annealing time (top-left), temperature (top-right) and Au film thickness (bottom-left). The Au films were thermally evaporated on Si wafers and annealed in air.

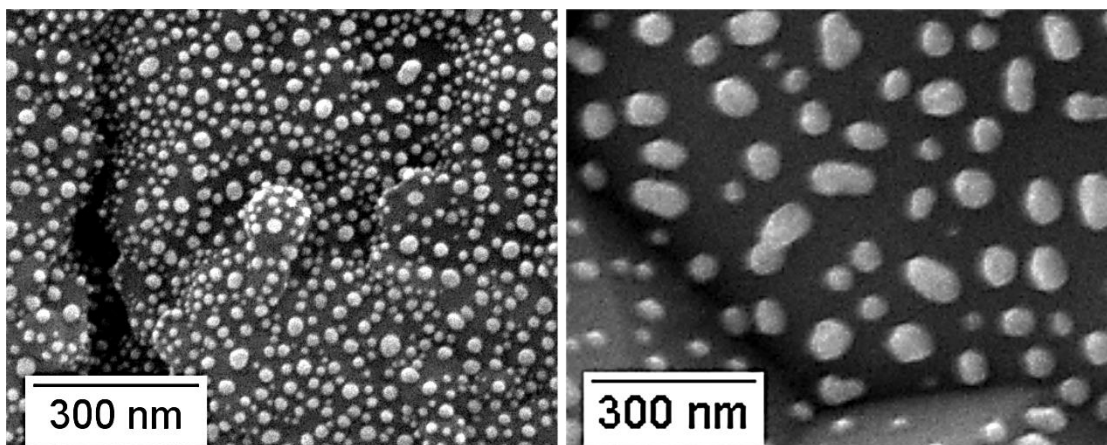


Fig. 5.15 3.7 nm Au on Mo (left) and 5.5 nm Au on CdTe-coated Mo foil (right). Both films were annealed at 360°C for 30 mins.

Comparison between samples with Au nanodot arrays on Si wafers and bare and CdTe-coated Mo foils (Fig 5.15) showed similar particle distribution trends with varying annealing temperature, time and film thickness. An increase in the average diameter and decrease in the average density having the same orders of magnitude was observed in nanodot arrays on bare and coated Mo foils. On the contrary, decreasing pressure values resulted in more dense arrays with smaller particles and having the same orders of magnitude. Generally, Au on Si results were more suitable for particle imaging analysis due to a smoother surface compared to the other substrates and were chosen to be shown here for which detailed statistical analysis was less feasible.

5.4.2 Morphology and elemental composition of CSS-grown Au-catalysed CdTe nanowires

CdTe nanowires were successfully fabricated on both bare and CdTe-coated substrates with the latter demonstrating a higher nanowire density. In this section, results on the elemental composition and the morphology of the nanowire arrays on CdTe-coated Mo foils are presented.

Fig 5.16a shows the morphology of a representative sample with CdTe nanowires grown on a CdTe-coated Mo foil. The Au catalysts were generated by annealing a 5.5

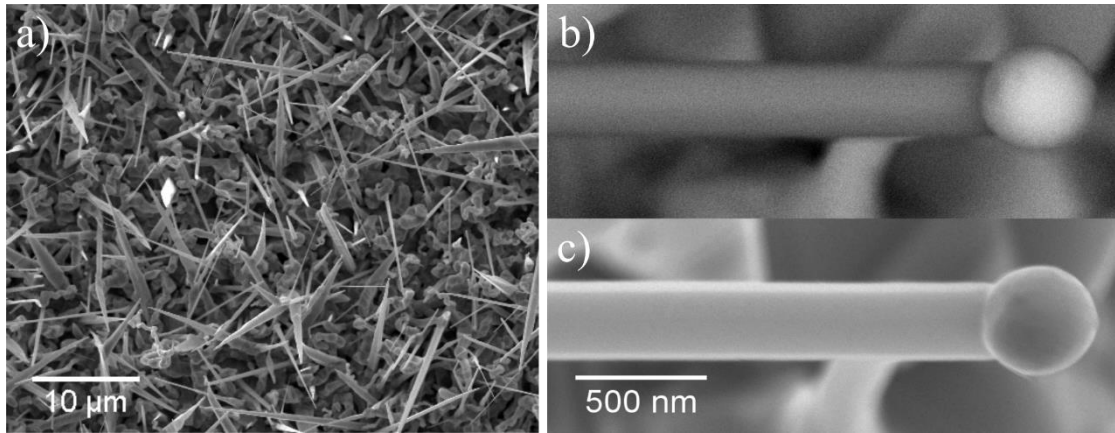


Fig. 5.16 a) Secondary electron SEM plan view of CdTe nanowires grown on a CdTe-coated Mo foil. The Au film (5.5 nm) annealing conditions were: $T_{src} = 360^{\circ}\text{C}$, $T_{sub} = 360^{\circ}\text{C}$, 300 Torr, 30 mins and the NW growth conditions: $T_{src} = 570^{\circ}\text{C}$, $T_{sub} = 540^{\circ}\text{C}$, 20 Torr, 20 mins. b) Back-scattered and c) secondary electron images of an individual CdTe nanowire.

nm thick Au film at 360°C under a static argon pressure of 300 Torr for 30 mins and, subsequently, changing the growth conditions to $T_{src} = 570^{\circ}\text{C}$, $T_{sub} = 540^{\circ}\text{C}$, 20 Torr, 20 mins. The generated nanowires had straight and tapered geometries, a random distribution of growth orientations, and lengths that varied from ~ 1 to $35\ \mu\text{m}$ and diameters from $\sim 100\ \text{nm}$ to $2\ \mu\text{m}$. Moreover, completely different worm-like randomly-oriented nanostructures with non-faceted sidewalls and rapidly varied growth directions were observed (Fig 5.17). These structures had a high density of kinks and diameter

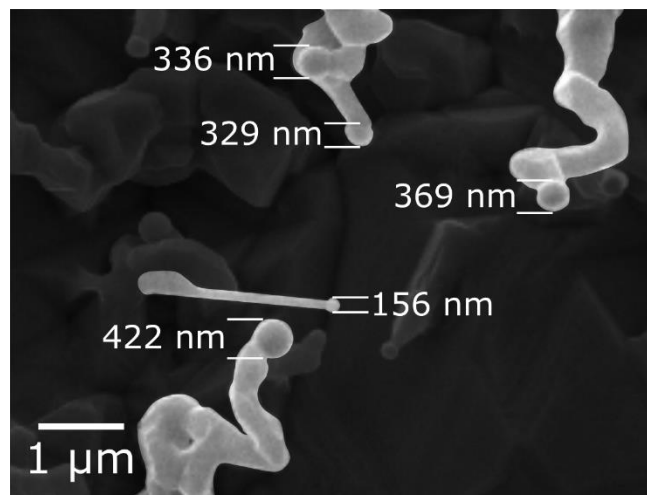


Fig. 5.17 Secondary electrons SEM image of worm-like nanostructures and a straight nanowire. Spherical droplets can be seen at the tips of both types of structures, with the nanowire one being considerably smaller.

Table 5.3 Average, minimum and maximum diameter values of nanowires and worm-like nanostructures. The data were acquired from all the samples used in this section.

	<i>N</i>	Avg diameter (nm)	Min diameter (nm)	Max diameter (nm)
Nanowires	484	153 ± 39	64	333
Worm-like nanostructures	452	314 ± 92	128	759

variations along their length. Spherical particles were observed at the tips of both the straight and worm-like nanowires. The average, minimum and maximum particle diameters were calculated from ~ 480 nanowires and 450 worm-like nanostructures as shown in Table 5.3. Catalyst droplets at the tips of the nanowires were found significantly smaller regardless growth conditions. High-magnification secondary and back-scattered electron images of the end of an individual straight nanowire are shown in Fig 5.16b and c. Since BSE contrast is compositional, not topographical, the bright droplet was assumed to be the Au catalyst and this was confirmed using SEM/EDX analysis (see below). The distribution of the nanowires length and diameter and catalysts size were obtained by analysing ~ 200 nanowires. Although a clear relation between nanowire length, diameter and catalyst size could not be established, tapered and thicker nanowires were longer than the straight and thin. The average nanowire density was $\sim 10^7 \text{ cm}^{-2}$ (calculated from the SEM micrographs), which is at least two orders of magnitude lower than the average density of the Au nanoparticles ($\sim 10^9 \text{ cm}^{-2}$).

The elemental compositions of a typical nanowire's trunk and tip were determined using SEM/EDX elemental analysis. Data were collected from five points with varied distance from the centre of the catalyst (Table 5.4) and the Au, Cd and Te content was plotted against the distance (Fig 5.18). The elemental analysis of the droplet was 77

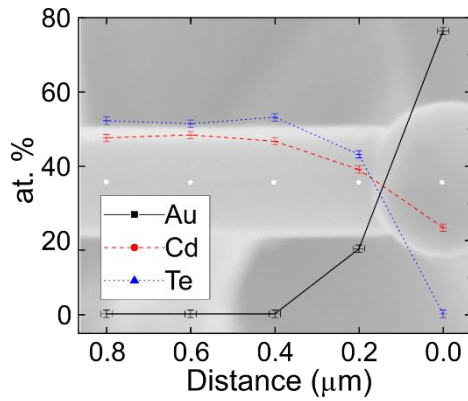


Table 5.4 Au, Cd and Te content for varying distances from the centre of the Au droplet.

Distance (nm)	Au (at.%)	Cd (at.%)	Te (at.%)
0	77	23	0
200	18	39	43
400	0	47	53
600	0	48	52
800	0	48	52

Fig. 5.18 Plot of the Au, Cd and Te content in the trunk and tip of an individual Au-catalysed CdTe nanowire. Background: secondary electron SEM image of the measured CdTe nanowire. The white circles denote the sites used for the SEM/EDX analysis. $E_{beam} = 15$ keV; the penetration range in Au is < 300 nm and in CdTe < 700 nm.

at.% Au and 23 at.% Cd. This confirms the hypothesis that such droplets at the nanowire tips are the remaining Au-rich catalysts. An exponential decrease of the Au content can be observed with increasing distance. At 200 nm from the droplet's centre, close to the tip – trunk interface, 18 at.% Au was detected, while no Au was detected in the nanowire trunk at 400 nm from the droplet's centre. However, resolution limitations of the SEM/EDX setup and possible signal contributions from nearby areas other than the examined nanowire may introduce measurement artefacts. The electron beam energy used in the measurement was 15 keV and a maximum electron penetration depth of ~ 300 nm in Au and ~ 700 nm in CdTe was calculated using the Casino Monte Carlo simulation software²⁸. Therefore, although the point measurements at the nanowire's trunk probably include instrumental errors up to a certain extent, the measured elemental composition of the droplet is less likely to be affected.

5.4.3 Investigation of the CdTe nanowire growth orientation

The $\theta - 2\theta$ XRD spectra of a planar and a NW CdTe buffer layer grown on Mo foils are shown in Fig 5.19. The spectrum of a bare Mo foil is included as a control. CdTe texture

coefficients and degree of preferred orientation of both the planar and the NW coated samples are presented on Table 5.5. JCPDS reference files 03-065-0880 (cubic CdTe), 00-019-0193 (hexagonal CdTe), 00-004-0809 (Mo) and 00-004-0784 (Au) were used to identify the diffractograms peaks.

In both samples, the highest intensity peak was the (111), which is typical for sputtered and CSS grown CdTe. However, the NW sample had a lower degree of preferred orientation (as seen from the lower spread of the texture coefficients compared to the planar sample). In particular, increases in the intensity of the (220), (331), (440) and (531) peaks were observed while peaks (111), (311), (400), (422) and (511) decreased with the strongest changes being for the (111) and (220) peaks. Overall, the CdTe NW sample was more randomly oriented than the planar sample. The lattice parameters of

Table 5.5 Texture coefficients and degree of preferred orientation of planar and NW coated CdTe samples. Planar: Mo foil/CdTe buffer layer, NW: Mo foil/CdTe buffer layer/CdTe NWs.

	$TC_{(111)}$	$TC_{(220)}$	$TC_{(311)}$	$TC_{(400)}$	$TC_{(331)}$	$TC_{(422)}$	$TC_{(511)}$	$TC_{(440)}$	$TC_{(531)}$	σ
Planar	2.01	0.22	0.9	1.75	0.67	1	1.51	0.25	0.69	0.63
NW	1.49	0.71	0.88	1.58	0.86	0.89	1.31	0.54	0.74	0.37

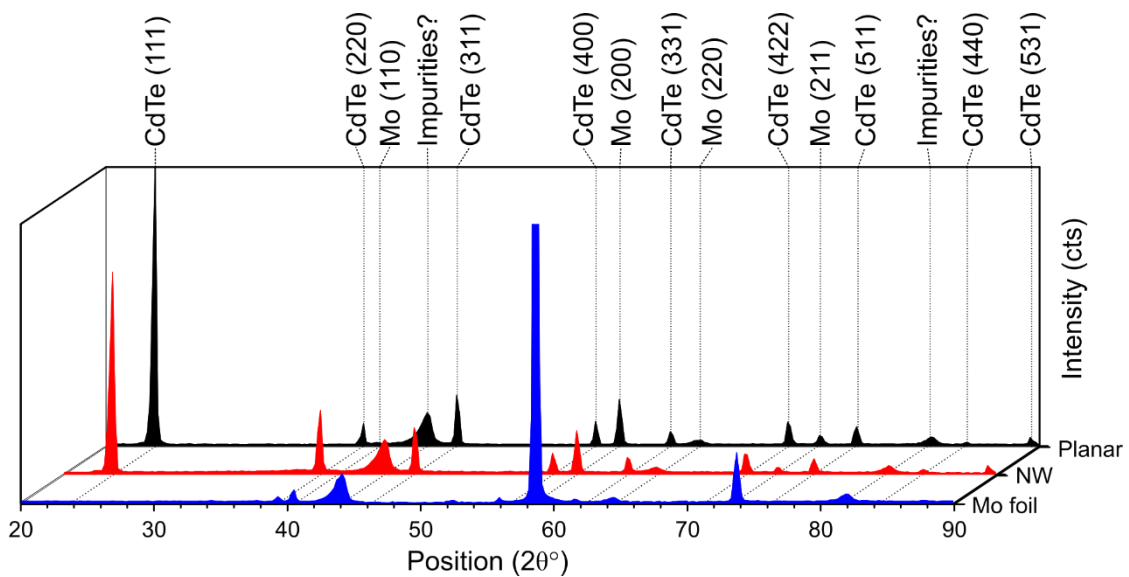


Fig. 5.19 XRD spectra of a Mo foil, a stack of Mo foil/CdTe buffer layer/CdTe NWs and a stack of Mo foil/CdTe buffer layer.

the planar and the NW CdTe samples were calculated from the position of the (111) peaks and were 6.478 ± 0.003 and 6.475 ± 0.003 Å respectively. These values are lower than the CdTe bulk value of 6.483 Å. This discrepancy can be ascribed to residual strain in the samples of this work or instrumental errors.

5.4.4 Effect of Au film thickness, deposition time, pressure and temperature on the growth of CdTe nanowires

Results on the morphology of the generated nanowire arrays for varying Au film thickness, deposition time, pressure and substrate temperature are presented here. All samples demonstrated right-skewed nanowire length and diameter distributions.

5.4.4.1 Impact of deposition time and Au film thickness

In Fig 5.20, SEM images of nanowire arrays generated by depositing CdTe for 5 and 20 mins on samples with varying Au film thicknesses (1.8, 3.7 and 5.5 nm) are shown. The Au films were deposited on CdTe-coated Mo foils and annealed at $T_{src} = 360^\circ\text{C}$, $T_{sub} = 360^\circ\text{C}$, 300 Torr, 30 mins and the nanowire growth conditions were: $T_{src} = 570^\circ\text{C}$, $T_{sub} = 530^\circ\text{C}$, 20 Torr. The dependence of the diameter and length distributions on the Au film thickness and deposition time is demonstrated in Fig 5.21. The three horizontal lines (top-to-bottom) of each box represent the 75th percentile, the mean and the 25th percentile values respectively and the boxplot sample size varied with the nanowire density of each sample. (For each bin, the individual data points are spread out horizontally in order to display all of the data without overlaps). The average nanowire density, diameter and length values as well as the catalyst size at the tips of nanowires (d_{cat}^{str}) and worm-like nanostructures (d_{cat}^{worm}) are shown on Table 5.6.

Despite the data spread, a general trend for the effect of Au film thickness on the nanowire morphology can be observed: thicker Au films generated arrays with shorter

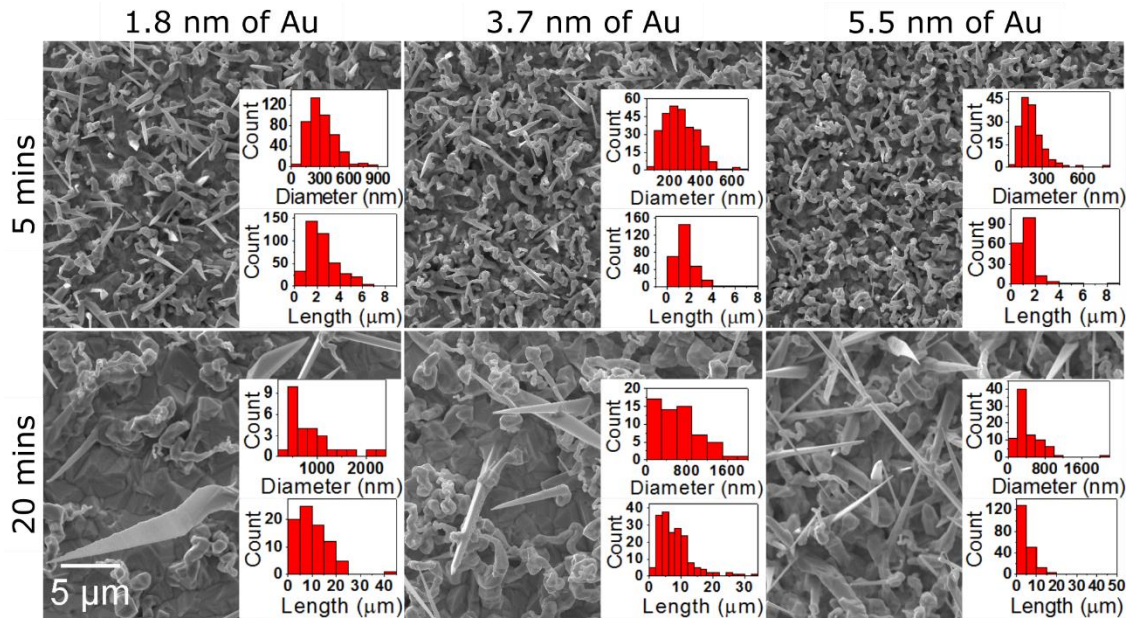


Fig. 5.20 Secondary electrons SEM images of CdTe nanowire arrays generated with varying CdTe deposition time and Au film thickness. Arrays with longer and thicker nanowires were observed with increasing deposition time and decreasing Au film thickness. Insets: nanowire length and diameter histograms.

and thinner nanowires. While a relation between d^{str}_{cat} and film thickness could not be inferred with certainty due to the very small variations in catalyst size with film thickness, the size of the catalyst at the tips of the worm-like nanostructures increased with the film thickness. Moreover, for increasing Au film thickness, while a decrease in the nanowire density was observed after 5 minutes of CdTe deposition, increasing densities were observed after 20 minutes. Nevertheless, the nanowire densities were at least two orders of magnitude lower than the average density of the Au nanoparticles

Table 5.6 Average nanowire density, diameter and length values for varying Au film thickness and deposition time.

Au (nm)	Time (mins)	Density (cm ⁻²)	Diameter (nm)	Length (μm)	d^{str}_{cat} (nm)	d^{worm}_{cat} (nm)
1.8	5	1.6×10^7	323 ± 147	2.5 ± 1.3	142 ± 38	219 ± 52
	20	1×10^6	888 ± 529	10.2 ± 6.4	147 ± 30	240 ± 63
3.7	5	1.1×10^7	269 ± 104	1.7 ± 1.1	144 ± 35	280 ± 78
	20	2.2×10^6	656 ± 412	8 ± 5.2	140 ± 41	250 ± 65
5.5	5	6.8×10^6	223 ± 90	1.4 ± 0.9	143 ± 30	334 ± 86
	20	3.1×10^6	437 ± 295	5.4 ± 9.4	135 ± 26	400 ± 54

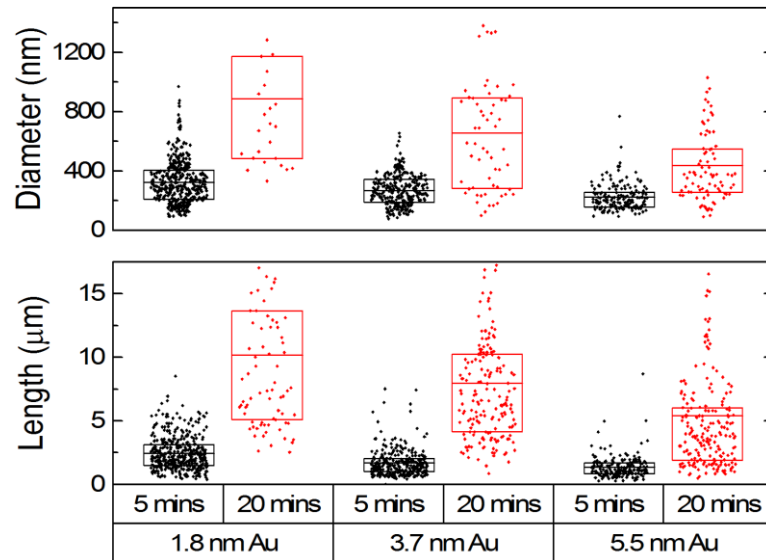


Fig. 5.21 Diameter and length boxplots of nanowire arrays for varying Au film thicknesses and deposition times. Increasing nanowire lengths and diameters were observed with increasing deposition time and decreasing Au film thickness.

before the nanowire growth ($\sim 10^9 \text{ cm}^{-2}$). A qualitative evaluation of the worm-like nanostructures density showed an increase in their density with Au film thickness.

Similar nanowire length and diameter variations with deposition time were observed for all samples regardless the Au film thickness. Thus, representative results for the 1.8 nm thick Au film samples are presented here. After 5 minutes of deposition, nanowire arrays ($\sim 1.6 \times 10^7 \text{ cm}^{-2}$) with average lengths of $2.5 \mu\text{m}$ and diameters of 323 nm were observed. At longer deposition times (20 minutes), the nanowire density decreased by an order of magnitude ($\sim 1 \times 10^6 \text{ cm}^{-2}$) and the nanowires had an average length of $10.2 \mu\text{m}$ and diameter of 888 nm. Moreover, while after 5 minutes of growth most of the nanowires were straight with small diameter variations with length, nanowire arrays that were generated after 20 minutes of CdTe deposition demonstrated more intense tapering effects. In extreme cases, the diameter – length decrease rate (base-to-tip) along the axis was $> 120 \text{ nm}/\mu\text{m}$. However, a relation between the catalyst droplet sizes for straight and worm-like NWs and deposition time could not be inferred.

5.4.4.2 Impact of deposition pressure and Au film thickness

Fig 5.22 shows SEM images of nanowire arrays generated by depositing CdTe under 20 and 40 Torr of N₂ on substrates with varying Au film thicknesses. The Au films were deposited on CdTe-coated Mo foils and annealed at $T_{src} = 360^{\circ}\text{C}$, $T_{sub} = 360^{\circ}\text{C}$, 300 Torr, 30 mins and the nanowire growth conditions were: $T_{src} = 570^{\circ}\text{C}$, $T_{sub} = 530^{\circ}\text{C}$ for 20 mins. Nanowire diameter and length distributions for samples with 1.8, 3.7 and 5.5 nm thick Au films grown under 20 and 40 Torr of N₂ are shown in Fig 5.23. The average nanowire density, diameter and length values as well as the catalyst size at the tips of nanowires (d_{cat}^{str}) and worm-like nanostructures (d_{cat}^{worm}) are shown on Table 5.7.

Regardless deposition pressure, all generated arrays had shorter and thinner nanowires with increasing Au film thickness. Moreover, the density (qualitative) and size of the worm-like nanostructure catalysts scaled proportionally with Au film thickness, while that of the nanowire catalysts inversely proportional. Overall, these findings are in accordance with the findings of Section 5.4.4.1. While the density of nanowires that

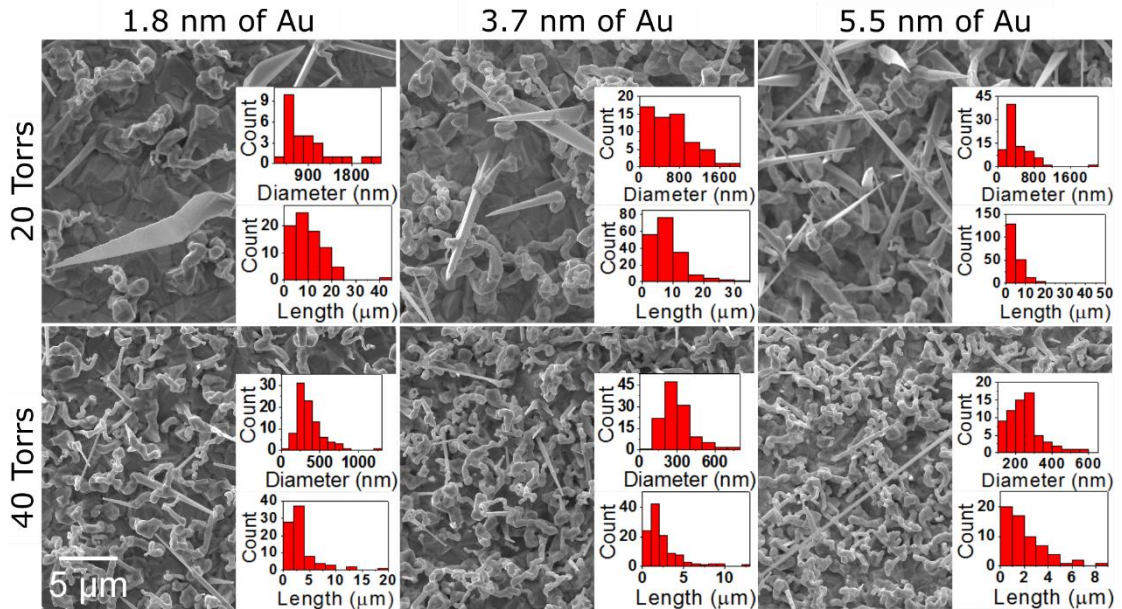


Fig. 5.22 Secondary electrons SEM images of CdTe nanowire arrays generated with varying CdTe deposition pressure and Au film thickness. Shorter and thinner nanowires were observed with increasing deposition pressure and Au film thickness. Insets: nanowire length and diameter histograms.

Table 5.7 Average nanowire density, diameter and length values for varying Au film thickness and deposition pressure.

Au (nm)	Pressure (Torr)	Density (cm ⁻²)	Diameter (nm)	Length (μm)	d_{cat}^{str} (nm)	d_{cat}^{worm} (nm)
1.8	20	1×10^6	888 ± 529	10.2 ± 6.4	147 ± 30	240 ± 63
	40	3.4×10^6	365 ± 181	3.4 ± 3	178 ± 41	298 ± 68
3.7	20	2.2×10^6	656 ± 412	8 ± 5.2	140 ± 41	250 ± 65
	40	4.4×10^6	304 ± 125	2.4 ± 2.2	170 ± 43	325 ± 82
5.5	20	3.1×10^6	437 ± 295	5.4 ± 9.4	135 ± 26	400 ± 54
	40	2.5×10^6	249 ± 95	2.2 ± 1.6	160 ± 36	366 ± 98

were generated under 20 Torr increased proportionally with the thickness of the Au film, a clear trend was not observed for samples that were fabricated under 40 Torr of nitrogen. Nevertheless, the nanowire densities were at least two orders of magnitude lower than the average density of the Au nanoparticles before the nanowire growth ($\sim 10^9 \text{ cm}^{-2}$), as observed in the earlier studies presented.

Increasing deposition pressures resulted in nanowire arrays with shorter, thinner and less tapered nanowires regardless Au film thickness. While a relation between deposition pressure and NW density could not be inferred, the number of worm-like

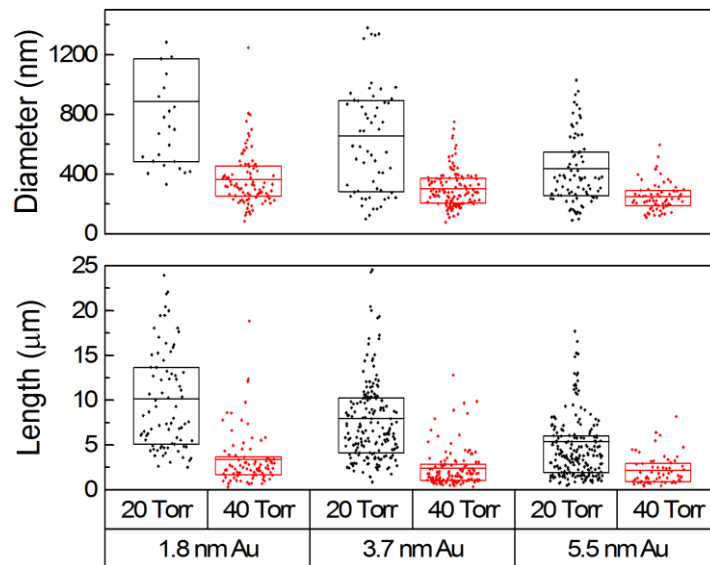


Fig. 5.23 Diameter and length boxplots of nanowire arrays for varying Au film thickness and deposition pressure. Decreasing nanowire lengths and diameters were observed with increasing deposition pressure and Au film thickness.

nanostructures seemed to increase (qualitatively) with deposition pressure. Overall, d_{cat}^{str} and d_{cat}^{wrm} increased with increasing deposition pressure.

5.4.4.3 Impact of substrate temperature

Fig 5.24 shows the effect of substrate temperature on the morphology of the CdTe nanowire arrays. Nanowires were generated at $T_{src} = 570^\circ\text{C}$ under 20 Torr for 20 mins, while the substrate temperature was in the range $530 - 560^\circ\text{C}$. The nanowire diameter and length distributions are shown in Fig 5.25. The average nanowire density, diameter and length values are shown on Table 5.8.

Increasing the substrate temperature during the CdTe growth produced NW arrays with greater NW aspect ratios and less tapered geometries. A significant number of nanowires with lengths exceeding $60\ \mu\text{m}$ were observed in samples generated at $T_{sub} > 550^\circ\text{C}$ using low magnification SEM images. On the contrary, the nanowires' diameter and density decreased with increasing substrate temperature.

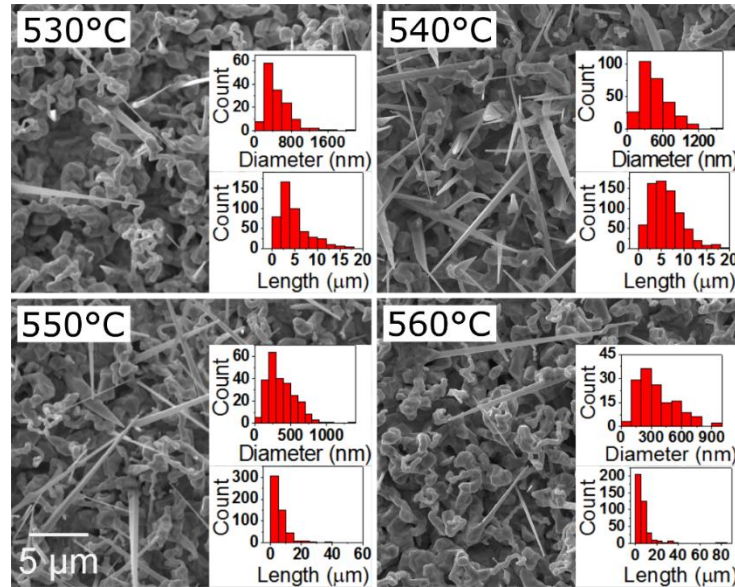


Fig. 5.24 Secondary electrons SEM images of CdTe nanowire arrays generated at $T_{src} = 570^\circ\text{C}$, $T_{sub} = 530 - 560^\circ\text{C}$, 20 Torr, 20 mins. Insets: nanowire length and diameter histograms.

Table 5.8 Average nanowire density, diameter and length values for varying substrate temperature.

Substrate temperature (°C)	Density (cm ⁻²)	Diameter (nm)	Length (μm)
530	1×10^7	495 ± 309	4.8 ± 3.4
540	1.1×10^7	474 ± 252	6 ± 3.4
550	9×10^6	371 ± 197	6.1 ± 6.1
560	5.3×10^6	356 ± 187	7 ± 7.9

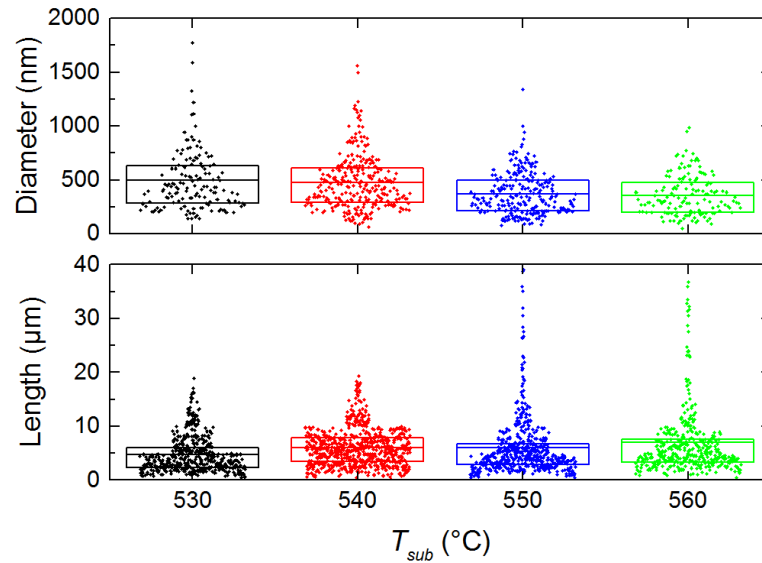


Fig. 5.25 Boxplots of nanowire diameter and length for varying substrate temperature.

5.4.5 Discussion of the Au-catalysed VLS growth of CdTe nanowires

5.4.5.1 Development of Au nanodot arrays

The development of Au nanodot arrays by thermally-induced de-wetting of Au thin films has been widely used and reported^{29–32}. As-grown thin films are usually metastable and can spontaneously de-wet under heating. The de-wetting process of metallic thin films on solid substrates is thermodynamically driven by the minimisation of the total surface energy of the ambient, film and substrate interfaces. Depending on the annealing conditions liquid or solid state de-wetting may occur.

Au nanodot arrays on Si wafers and Mo foils were successfully generated in the 300 – 500°C temperature range. Since the melting point of Au is 1064°C and the eutectic

points in the Au – Si and Au – Mo systems are at 360 and 1054°C respectively, it is speculated that the nanodot arrays were formed via a solid state de-wetting process. Solid state de-wetting proceeds via surface diffusion and can occur at temperatures well below the melting point of the thin films, which decrease with film thickness^{31,33,34}. Moreover, weak substrate – film interactions, as in Au films on Si/SiO₂ wafers, can lower the activation energy for metal atom migration and increase the rate of dewetting³⁵. SEM micrographs of as-deposited Au films (Fig. 5.13) showed high densities of grooves on the surface of the samples. It is speculated that such grooves may promote void nucleation and lead to film de-wetting and the formation of nanodots. Moreover, the linear hydrodynamic spinodal de-wetting theory for liquid films suggests that the particle-to-particle distance and the mean particle diameter vary proportionally to t^2 and $t^{5/3}$ respectively, where t is the film thickness^{36,37}. In this work, such proportionalities were not observed. Lastly, size- and pressure-induced melting point depression effects were ruled out as having insignificant impact for the experimental conditions in this work.

Increasing annealing times and temperatures had a similar effect on the morphology of the generated Au nanodot arrays: a minimum average nanodot diameter and a maximum average density was observed after 45 mins at 300°C or 30 mins at 400 – 450°C (5.5 nm thick films). Further increase in the annealing time or temperature led to nanodot arrays with larger particles and lower densities. This can be ascribed to coalescence of the nanodots under these annealing conditions. Particles' coalescence due to prolonged annealing of the Au films may be a result of Ostwald ripening and temperature-induced coalescence can be ascribed to longer diffusion lengths, which lead to the formation of larger nanodots. Considering the nanodots as spherical-shaped particles, larger nanodots are expected to have higher volume-to-surface (cross-sectional) ratio than the

smaller ones. Thus, nanodot arrays with a maximum surface coverage and density values were observed in samples with the smallest nanodots.

The initial Au film thickness was the parameter with the strongest effect on the de-wetting process and the characteristics of the nanodot arrays. Increasing the film thickness from 1.2 to 5.5 nm resulted in a 10-fold increase in nanodot diameter. In thin films, the high density of surface grooves can result in easier nucleation of voids, which tend to be more closely spaced than in thicker films. This is in accordance with the findings of Presland *et al*³⁸, showing that the number of holes during de-wetting decreases for thicker films. Moreover, Jiran and Thompson studies³⁹ on the agglomeration of continuous films have shown a dramatic decrease in the growth rate of voids with increasing film thickness. Lastly, a higher de-wetting rate is expected in thinner films due to a higher surface-to-volume ratio.

Annealing experiments under pressures ranging from 300 Torr (CSS chamber) to 760 Torr (box furnace) showed that film rupture occurred more readily at lower pressures. Studies on the effect of ambient pressure on the contact angle of droplets^{40,41} have shown that the contact angle scales with the ambient pressure. The contact angle of a droplet depends on the surface energies at the film – substrate and film – vapour interfaces. Thus, at lower contact angles (under lower pressures), a decrease in the surface energy at the film – vapour interface is expected. This results in a decrease of the total energy of the droplet – substrate – ambient system, considering that the substrate's surface energy remains constant. Therefore, since the driving force of the de-wetting process is the minimisation of the surface energies, film rupturing was faster at lower pressures.

Annealing experiments on Si wafers and CdTe-coated and bare Mo foils using the same conditions showed that the nanodot arrays that were generated on the Si wafers had smaller diameters than the ones on the Mo foils. This can be ascribed to differences in the surface properties, such as surface chemistry and roughness, between the Si wafers and the (un)coated Mo foils. An additional factor that can influence the de-wetting process in these experiments is the poor adhesion of Au on oxidised silicon due to its low sticking coefficient. According Gadkari *et al*⁴², a combination of poor adhesion and stress effects in Au films deposited on SiO₂ leads to the formation of delamination blisters and to a decrease in the activation energy for void nucleation and subsequent de-wetting. Lastly, as mentioned above, the poor Au – SiO₂ interaction leads to higher metal atom migration lengths and increases the rate of de-wetting.

5.4.5.2 Growth mechanism of the Au-catalysed CdTe nanowires

One factor that has a strong effect on the catalysed-fabrication of nanowires is the catalyst state during growth. Nanowires with different morphologies may grow using either the vapour – solid – solid (VSS)⁴³ or vapour – liquid – solid methods at different temperatures. Yet, determining which of the two growth modes prevailed is often difficult.

Au-catalysed nanowires fabricated in this work bared Au spherical droplets at the tips, which is generally considered as an indication to the VLS growth mode^{44–46}. SEM/EDX microanalysis at various points along the droplet and the trunk of the nanowires showed a high concentration of Au in the droplet, which decreased exponentially with increasing distance from the droplet's centre. No Au was detected in the nanowire trunk at distances > 200 nm from the droplet – nanowire interface. These indications of VLS growth mechanism are further amplified by the fact that the catalysts have a spherical

shape with diameters significantly larger than that of the nanowire trunk at the catalyst – nanowire interface⁴⁷. On the contrary, high concentrations of impurities in the catalyst are indicative of VSS grown nanowires⁴⁸, while in VLS a pure metal catalyst is expected^{49,50}. In this work, 23 at.% of Cd was detected in the catalyst after nanowire growth, which is not easy to reconcile with the Au – Te driven growth mechanism discussed below. Lastly, the growth conditions used in this work are very similar to the ones reported by Williams⁵¹ in a comprehensive study of the VLS growth of Au-catalysed CdTe nanowires. Conclusively, the experimental conditions used and the nanowires morphology in this work suggest that the nanowires were fabricated using the VLS growth mode.

The early stages of the proposed VLS growth mechanism for the nanowires generated in this work (alloy formation, crystal nucleation and nanowire growth) are now discussed. One prerequisite for the VLS growth to proceed is the existence of catalysts in the liquid state under growth conditions. According to the CdTe – Au phase diagram⁵¹ a eutectic point exists at 810°C (in standard equilibrium conditions), which is much higher than the temperatures used for the nanowire growth (520 – 560°C). This suggests that the Au catalysts are in the solid state initially. However, both Au – Cd and Au – Te systems^{52,53} have eutectic points at temperatures well below the growth temperatures. At 520°C, an excess of ~ 68 at.% Cd or 50 at.% Te is required in order for the Au – Cd or Au – Te binary compound to enter the liquid state. Furthermore, a liquid Au – AuTe₂ phase exists at 447°C at 52 at.% Te. Thus, it is speculated that in the initial stages of growth, liquid catalysts are formed by the diffusion of Te atoms in the Au islands. Nanowire growth proceeds as Cd atoms diffuse into the saturated Au – Te droplets, they bind with the Te atoms and CdTe layers precipitate. This model is in agreement with Williams⁵¹ findings and can explain the more readily growth of nanowires in samples

with CdTe-coated substrates, since the diffusion of Cd and Te atoms in the catalyst droplets can be achieved faster. Moreover, Di Carlo *et al*⁵⁴ have recently shown that the Au-catalysed VLS growth of CdTe nanowires by means of metalorganic vapour phase epitaxy can be controlled by adjusting the Te and Cd supply: initially, Au – Te droplets were formed by exposing the Au catalysts to a Te flux. Next, the chamber was purged to remove any unreacted Te compounds and nanowire growth was achieved by using only a Cd flux. Nevertheless, direct evaluation of the postulated model in the initial stages of the nanowire growth would require *in situ* EDX microanalysis.

5.4.5.3 Morphology of the CdTe nanowire arrays

In this section, the characteristics of the nanowire arrays are discussed.

Nanowire density: The average NW density was in the range of $\sim 10^6 - 10^7 \text{ cm}^{-2}$, which is at least two orders of magnitude lower than that of the Au nanodot arrays. As discussed, VLS growth of nanowires becomes favourable only when Au – Te liquid catalysts are formed and become saturated with Cd atoms. Therefore, it is highly probable that the growth of a thin CdTe film precedes the nanowire growth which may result in the burial of the Au nanodots up to some extent. Moreover, as shown in Section 5.4.1, the breadth of the diameter distribution of the Au nanodots can be greater than 100 nm. Thus, since NW growth proceeds upon the saturation of the catalysts with the semiconductor material, the growth rate is expected to decrease with catalyst size and even terminate above certain diameters. Other factors that may influence the nanowire density is catalyst coalescence, migration or incorporation at the nanowire growth temperatures.

Nanowire length – diameter relation: As shown in Section 3.2.2.2, adatoms can reach the catalyst during VLS growth by either direct impingement or surface diffusion.

Depending on which of the two routes dominates the process, nanowires with different aspect ratios and morphologies can be generated. In the case that direct impingement dominates the growth, thinner nanowires tend to grow slower because of the Gibbs – Thomson² effect^{55,56}. On the contrary, in cases where surface diffusion dominates, the nanowire length is inversely proportional to the diameter^{4,57,58}. In this work, due to significant tapering effects and wide distributions of nanowire lengths and diameters, a clear relation between nanowire length, diameter and catalyst size could not be inferred. However, only thick (tapered) nanowires with diameters $> 1 \mu\text{m}$ were observed exceeding $10 \mu\text{m}$ in length. Therefore, it is postulated that the major contribution in the NW growth was either the direct impingement or an interplay between direct impingement and the surface diffusion of the Cd and Te adatoms.

Nanowire tapering: The nanowire arrays that were generated comprised straight and tapered nanowires. In general, tapering effects in nanowires grown by the VLS method occur due to instability and gradual volume reduction of the catalyst through diffusion, incorporation, evaporation or reaction phenomena^{3,59} and the uncatalyzed vapour – solid growth on the nanowire sidewalls^{56,60}. Although the former case may be valid for the nanowires in this work up to a certain extent, it is less probable, since a termination of the VLS growth is expected for long deposition times. On the contrary, catalyst droplets were observed at the tips of most of the nanowires even after 60 mins of CdTe deposition. Thus, the nanowire tapering in this work is more likely to have happened due to the uncatalyzed vapour – solid deposition on the sidewalls. This is in accordance

² The Gibbs – Thomson effect predicts that the supersaturation of the alloy catalyst, which is the driving force in VLS nanowire growth, decreases with the droplet diameter.

with the fact that tapering effects were more significant in longer nanowires, where the diffusion length of the Cd and Te adatoms is smaller than the nanowire length.

Nanowire orientation: The well-defined diffraction peaks of the XRD spectra of the CdTe buffer layer and the CdTe buffer layer/NW stack imply a high order of crystallinity in both samples. However, the NW sample demonstrated a lower degree of preferred orientation. Although non-epitaxial growth of nanowires and nanowire kinking may lead to reflections from planes other than (111), it is postulated that the main contribution was the recrystallisation of the CdTe buffer layer that existed in both samples. At this point, one should take into consideration that the measured peak intensities compromise Bragg reflections from both the nanowires and the underlying CdTe buffer layer due to the penetration of the X-rays and the porosity of the nanowire layer. Indeed, the X-ray penetration depth was calculated using the HighScore Plus software⁶¹ (Cu K α radiation, $\rho_{\text{CdTe}} = 5.85 \text{ g/cm}^3$) and was 3.251 μm at an incident angle of 11.87° (111) and 11.103 μm an incident angle of 44.66° (531). Thus, the lower degree of preferred orientation of the NW sample can be ascribed to recrystallisation of the CdTe buffer layer during the NW growth (540°C, 20 mins), which is in accordance with Refs ^{62–64}.

Worm-like nanostructures: All samples regardless growth conditions comprised both nanowires and worm-like nanostructures and spherical droplets were observed at the tips of both. Kim *et al*⁶⁵ have ascribed the formation of worm-like tips in Au-catalysed VLS grown Si nanowires to Au wetting and instability phenomena. Similar worm-like morphologies have been reported by Govatsi *et al*⁶⁶ in an Au-catalysed VLS growth study of ZnO nanowires, where the density of such nanostructures scaled with Au film

thickness. This is in accordance with Hoffman's findings on the worm-like nanostructures during the Au-catalysed growth of Si nanowires⁶⁷. According to their findings, slower achievement of supersaturation and catalyst instability phenomena in larger droplets are responsible for the worm-like growth. Zannier *et al*⁶⁸ have shown that a switch from VLS to VSS growth mode during the catalysed growth of ZnSe NWs resulted in kinked, worm-like morphologies. In particular, it was achieved by controlling the Zn/Se ratio. In this work, the density of worm-like nanostructures increased with Au film thickness. Moreover, while the average catalyst diameter at the tips of the nanowires was 153 ± 39 nm and ranged between 64 and 333 nm, the average diameter of the catalysts at the tips of the worm-like nanostructures was 314 ± 92 nm and varied from 128 to 759 nm. As mentioned above larger catalysts require higher semiconductor material for supersaturation. Moreover, according to Di Carlo⁵⁴ an increase of the melting point of the ternary Au – Cd – Te may occur with increasing Cd concentrations, which may shift the growth mechanism from VLS to VSS. Thus, it is speculated that the worm-like growth is due to a combination of slow supersaturation and an interplay between the VLS and VSS growth mechanisms that occur in larger catalysts.

5.4.5.4 Effect of Au film thickness, deposition time, pressure and temperature on the growth of CdTe nanowires

Effect of Au film thickness: As shown in Section 5.4.1, thicker Au films resulted in less dense and bigger nanodots. Since the NW growth depends directly on the density and size of the catalyst arrays, a similar density – diameter trend was expected for the generated NW arrays. Nevertheless, increasing Au film thickness resulted in a) less dense NW arrays after 5 mins and b) more dense NW arrays after 20 minutes of CdTe deposition under 20 Torr of pressure, while no clear trend was observed after 20 minutes

of CdTe deposition under 40 Torr of pressure. Regardless of the deposition conditions, the NW diameters decreased with Au film thickness. At the same time, the density of the worm-like nanostructures always increased with film thickness. Moreover, the size of the catalysts at the tips of the nanowires decreased, while that of the worm-like nanostructures increased with Au thickness. The discrepancy between the expected and the generated morphologies can be explained by considering, that in this work, only small catalysts with average diameters of 153 ± 39 nm resulted in successful NW growth, while the bigger ones with average diameters of 314 ± 92 nm generated only worm-like nanostructures. Therefore, the morphology trends in thicker Au films, where the number of big particles increases at the expense of small, can be ascribed to slow catalyst supersaturation, catalyst instability and changes in the growth mechanism (VLS vs VSS) as discussed above.

Effect of deposition time: As proposed in 5.4.5.2, during the early stages of CdTe deposition, Te adatoms diffuse in the Au nanodots forming Au – Te alloys and steady-state nanowire growth proceeds by the supersaturation of the catalysts with Cd adatoms. In this way, nanowires were generated after 5 minutes of deposition time with maximum lengths exceeding 1 μm . Longer CdTe deposition times resulted in lower nanowire densities, thicker, longer nanowires and more intense tapering effects. As discussed in 5.4.5.3, an increase of the nanowire length and diameter is expected for increasing deposition times during the VLS growth mode. Moreover, longer nanowires tend to have tapered geometries because their length exceeds the surface diffusion lengths of the Cd and Te adatoms and, thus, lateral growth occurs. Finally, the reduction in nanowire density can be ascribed to phenomena related to preferential nanowire growth directions or catalyst migration and incorporation during growth.

Effect of deposition pressure: Increasing deposition pressure resulted in more dense arrays with less tapered, shorter and thinner nanowires. At high deposition pressures, the vapour flux of Cd and Te adatoms that reaches the catalysts is reduced. This is because the number of collisions between the sublimated Te and Cd atoms and the N₂ molecules of the buffer gas scales with pressure. Thus, the flow of Cd and Te atoms is impeded and fewer Cd, Te adatoms with lower kinetic energies arrive to the sample's surface. Under these conditions, the flux of adatoms that diffuse in the catalysts is decreased, which in return results in decreased nanowire growth rate. Termination of the VLS growth is expected at even higher pressures, where the supersaturation of the catalysts is not possible. Kodambaka *et al*⁶⁹ have shown that the tapering effects in Au-catalysed Si NWs due to catalyst migration³ can be controlled by adjusting the oxygen partial pressure in the growth chamber. It was demonstrated that even slight changes in oxygen exposure result in immediate and dramatic effects on the growth kinetics and the morphology of the generated nanowires. This was ascribed to the formation of oxides during growth that can suppress the Au migration by reducing Ostwald ripening. Although, in this work only high purity N₂ was used as a buffer gas during growth, oxygen impurities in the CSS chamber are expected due to the CSS being a low – medium vacuum process and possible chamber leaks. Thus, changes in pressure may alter the oxygen content and, thus, can influence the nanowire growth.

Effect of substrate temperature: Lower temperature gradients between the source and the substrate are expected to result in lower incoming CdTe vapour flux and higher rates of CdTe resublimation at the substrate. This would suggest a decrease in the nanowire growth rate. On the contrary, higher substrate temperatures facilitate a lower requirement of diffused Cd and Te atoms in the catalyst for it to enter the

liquid state and become supersaturated³, which implies that nanowires can grow more readily. Meantime, surface diffusion of adatoms is a thermally activated process and increases with temperature. Increasing substrate temperatures enables the adatoms to diffuse to longer lengths, which enhances the surface diffusion contribution of the VLS nanowire growth. Thus, longer, thinner and less tapered nanowires are expected due to suppression of the uncatalysed sidewall nucleation and lateral growth. Lastly, axial and lateral growth of existing nanowires can be more favourable than the nucleation of new nanowires. Overall, it is speculated that the lower densities of nanowires having greater aspect ratios and less tapering that were generated at higher substrate temperatures were the result of a combination of these diffusion processes.

5.5 Growth of CdTe nanowires using Bi catalysts

5.5.1 Development of Bi nanodot arrays

Results on the de-wetting of Bi thin films and the generation of nanodot arrays are presented here. The annealing process was carried out in a) a static N₂ ambient and b) a dynamic H₂/N₂ ambient. First, results using the static N₂ ambient are presented.

5.5.1.1 Annealing in N₂ ambient

Fig 5.26 shows secondary electrons SEM images of as-grown Bi thin films (1, 2 and 3 nm thick) on a Si wafer. Bi nanodots with densities in the 10¹¹ cm⁻² range and diameters which scaled with film thickness can be seen. The average diameters were: 14 ± 4 nm,

³ Namely, at 520°C the solidus line of the Au – Te system is crossed at ~ 50 at.% Te and that of the Au – Cd system at ~ 68 at.% Cd, while at 560°C the solidus line of the Au – Te system is crossed at ~ 47 at.% Te and that of the Au – Cd system at ~ 60 at.% Cd

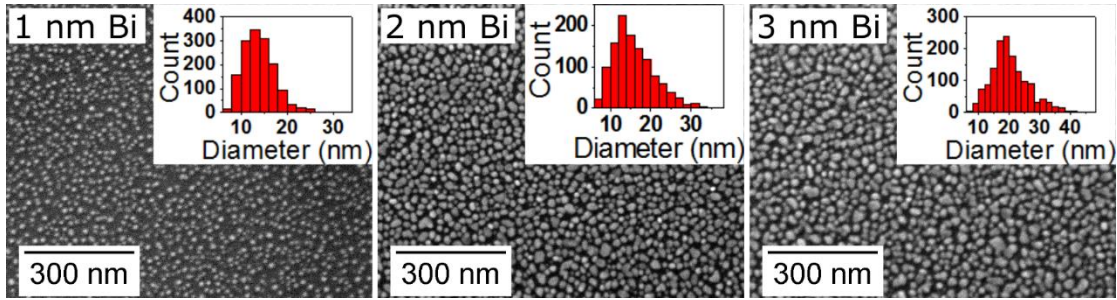


Fig. 5.26 As-grown Bi films of varied thickness (1, 2 and 3 nm) on Si wafers. Insets: nanodot diameter histograms.

16 ± 5 nm and 20 ± 6 nm. The interparticle distance decreased with increasing film thickness and films with thicknesses greater than 5 nm were more compact with surface coverage $> 80\%$. The de-wetting of thick Bi films and the formation of nanodot arrays was investigated by annealing 7 nm thick films at $300 - 500^\circ\text{C}$ under 5 Torr of nitrogen (static) for 60 mins (Fig 5.27). As shown in the SEM micrographs, even at 400°C the films remained almost unchanged and film de-wetting did not occur regardless annealing temperature. At 500°C , smearing of the surface morphology was observed. Similar results were obtained by annealing Bi films on bare and CdTe-coated Mo foils regardless annealing conditions. It was speculated that film de-wetting was impeded by the formation of oxides on the surface of the bismuth films before and/or during the annealing process. Therefore, the annealing and de-wetting of thin bismuth films in a reducing H_2/N_2 ambient was investigated and is presented below.

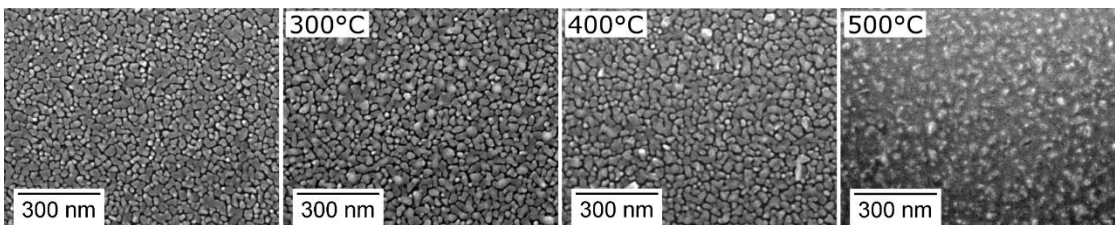


Fig. 5.27 Secondary electron SEM images of Bi films (7 nm) on Si wafers. The films were annealed under 5 Torr of nitrogen for 60 mins at $300 - 500^\circ\text{C}$. Film dewetting and the generation of nanodot arrays could not be observed regardless annealing temperature.

5.5.1.2 Annealing in H_2 ambient

Annealing of Bi films (4 nm) on Mo foils (400°C, 30 Torr, 10 mins) in a H_2/N_2 ambient (30 sccm H_2 , 20 sccm N_2) resulted in the generation of well-defined spherical Bi nanodots with average diameters of 43 ± 31 nm and an average density of $\sim 10^{10} \text{ cm}^{-2}$ (Fig 5.28). Bi nanodot arrays were obtained with lower H_2 content, but the particles were faceted and not well-defined.

Fig. 5.29 shows secondary electrons SEM images of Bi thin films (7 nm thick) on Si wafers annealed at 350 – 450°C under 30 Torr of H_2/N_2 (30/20 sccm) for 10 mins. The average density and diameter values are shown in Table 5.9 and Fig. 5.30. As can be seen, increasing the annealing temperature resulted in arrays with larger particles and lower densities.

The relation between the bismuth film thickness and average particle diameter and interparticle distance was investigated by annealing 5, 6 and 9 nm thick films at 450°C

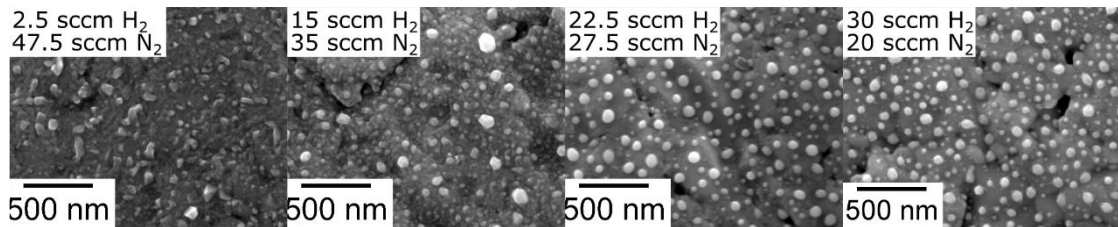


Fig. 5.28 Secondary electron SEM images of Bi films (4 nm) on Mo foils. The films were annealed under 30 Torr of H_2/N_2 (5 – 60% H_2) for 10 mins at 400°C. Increasing H_2 content led to the formation of nanodot arrays by impeding the effects of oxidation phenomena.

Table 5.9 Average Bi nanodot density and diameter values for varying annealing temperature. The Bi films (7 nm) were deposited on Si wafers and annealed under 30 Torr of H_2/N_2 (30/20 sccm) nitrogen for 10 mins.

Annealing temperature (°C)	Density (cm^{-2})	Diameter (nm)
350	1.3×10^{10}	36 ± 32
400	5.4×10^9	58 ± 36
450	7.3×10^8	126 ± 84

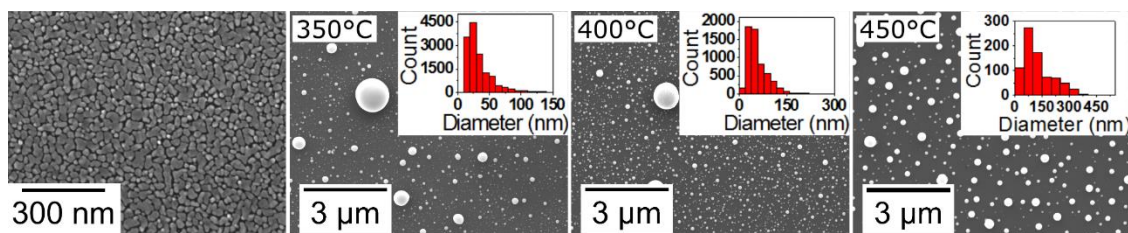


Fig. 5.29 Secondary electron SEM images of Bi films (7 nm) on Si wafers. The films were annealed under 30 Torr of H_2/N_2 (30/20 sccm) for 10 mins. Increasing annealing temperatures promoted the formation of small particles initially, which coalesced into larger particles at higher temperatures. Insets: nanodot diameter histograms.

under 30 Torr of H_2/N_2 (30/20 sccm) for 10 mins. The obtained diameter and interparticle distance values were plotted against film thickness and are shown in Fig 5.31. As discussed in Section 5.4.5.1, the linear hydrodynamic spinodal de-wetting theory for liquid films suggests that the particle-to-particle distance and the mean particle diameter vary proportionally to t^2 and $t^{5/3}$ respectively, where t is the film thickness^{36,37}. In this work, the data were fitted using the allometric power function $y = ax^b$ and the mean particle diameter and particle-to-particle distance varied proportionally to $t^{1.8}$ and t^2 respectively. Although the convergence of the fits was acceptable and the values are in a very good agreement with the theoretical values, these

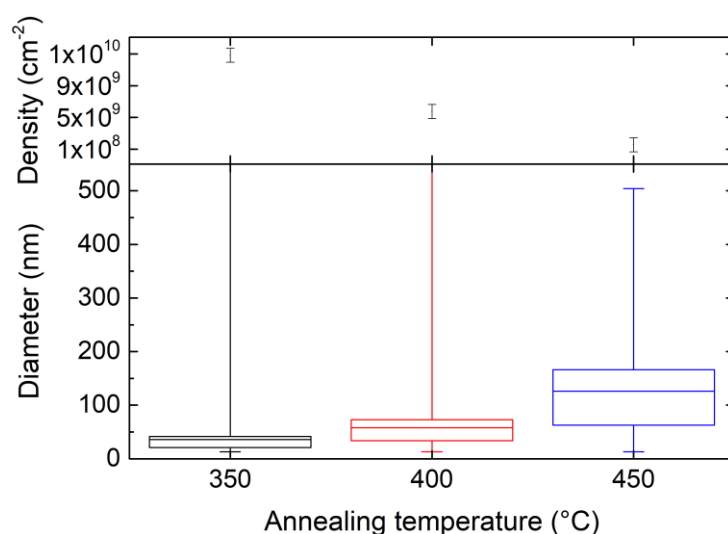


Fig. 5.30 Variation of the average nanodot density and diameter of Bi nanodot arrays with annealing temperature. The Bi films were thermally evaporated on Si wafers and annealed under 30 Torr of H_2/N_2 (30/20 sccm) nitrogen for 10 mins.

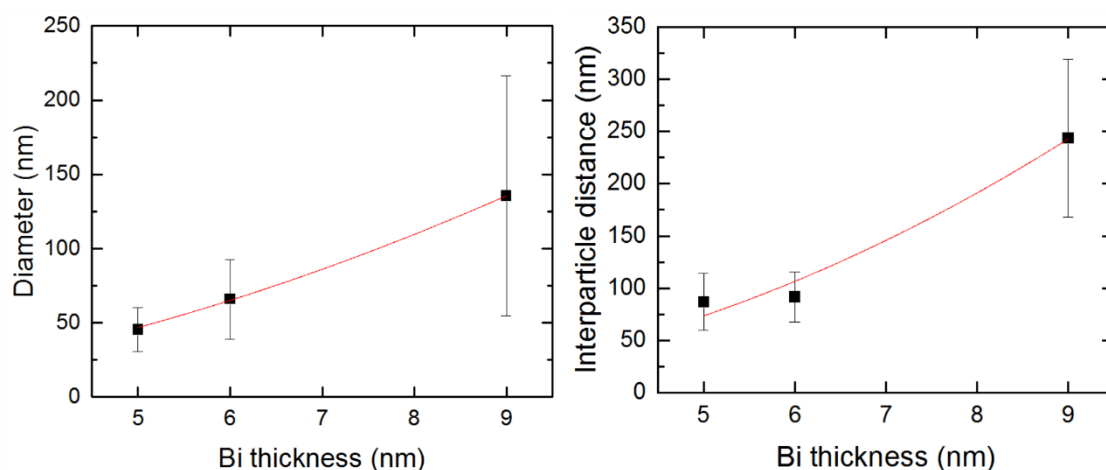


Fig. 5.31 Plots of average diameter and interparticle distance values against Bi film thickness. The red lines are fits of the allometric power function $y = ax^b$ and b was ~ 1.8 for the first plot and ~ 2 for the second.

proportionalities are subject to measurement errors due to the limited number of data points and the relatively broad standard deviation values of the measured quantities. Therefore, the formation of the Bi nanodot arrays by a liquid state de-wetting mechanism cannot be inferred with certainty. For a more detailed description of the liquid and solid state dewetting mechanisms the reader is referred to the discussion on the development of Au nanodots of Section 5.4.5.1.

5.5.2 Nanowire growth in N_2 ambient

As shown in Section 5.5.1.1, de-wetting of Bi films in a static N_2 ambient was impeded, probably due to surface oxidation effects. Nevertheless, CdTe nanowires were obtained using a narrow range of conditions. Specifically, 7 nm thick Bi films were deposited on CdTe-coated Mo foils, annealed at $T_{src} = T_{sub} = 400^\circ\text{C}$ under 5 Torr of N_2 for 10 mins and CdTe growth was carried out at 500°C , 5 Torr of N_2 with the substrate heater being turned off. SEM secondary electrons images of five samples after 5 – 60 mins of CdTe growth are shown in Fig 5.32. In the early stages of CdTe growth (5 – 10 mins), the nucleation of spontaneous CdTe islands was observed. After 20 – 40 mins, vertical

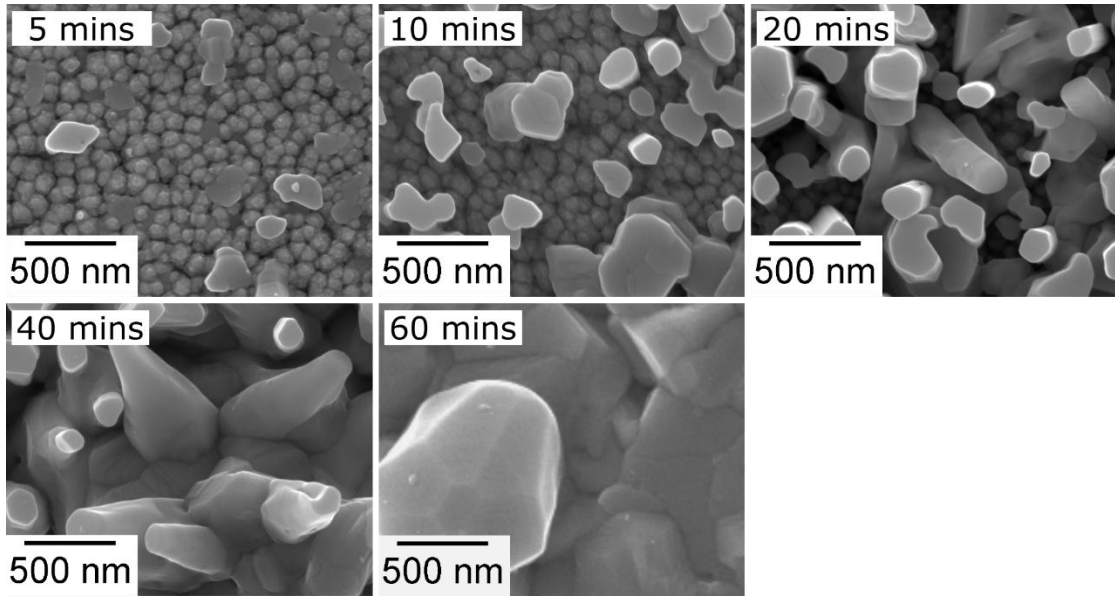


Fig. 5.32 Secondary electrons SEM images demonstrating the time evolution (5 – 60 mins) of the growth of CdTe nanowires in a static N_2 ambient. Annealing of Bi films (7 nm) was carried out at $T_{src} = T_{sub} = 400^\circ\text{C}$, 5 Torr, 10 mins and CdTe growth at $T_{src} = 500^\circ\text{C}$, 5 Torr (substrate heater off).

growth of the islands resulted in the formation of columnar structures of random cross-sections, diameters and lengths. Moreover, catalyst droplets could not be observed at the tips of the NWs at any point of the nanowire growth process. For longer CdTe growth times (> 60 mins), rough CdTe films without nanowires on their surface were observed. The effect of Bi on the nanowire growth was evaluated by repeating the same experimental procedure on Bi-free samples. In this case, CdTe growth resulted in the formation of ‘standard’ CdTe CSS-deposited thin films. Nevertheless, due to the limited control over the nanowire growth and geometries, nanowire growth in N_2 atmosphere was not further investigated.

5.5.3 Nanowire growth in H_2 ambient

In this section, results on the growth of bismuth-grown CdTe nanowires depicting a wide range of different geometries are presented. This was achieved by depositing thin Bi films on glass substrates and subsequent exposure to a CdTe vapour flux in H_2

ambient. However, while the use of H_2 was essential in impeding the oxidation of the Bi catalysts (Section 5.5.1.2), its use caused instability in the CSS CdTe source - which then caused irreproducibility in the growth conditions for NWs from run to run. An extensive range of growth conditions was explored in order to overcome the reproducibility issue but no simple experimental solution could be found. In this section, results on the morphology and the elemental composition of the nanowire arrays are presented.

5.5.3.1 Morphology and elemental composition of Bi-catalysed CdTe nanowires

NW growth was achieved for source and substrate temperatures that ranged from 480°C to 550°C and 400°C and 490°C respectively and no growth was observed outside these temperature regimes. In Fig 5.33, nanowires with rectangular (a) and hexagonal (b) cross-sections, as well as nanowires with sidewalls that exhibited periodic sawtooth faceting (c, d) are shown. The generated nanowires had straight and tapered geometries and a random distribution of growth directions. More intense sidewall tapering and sawtooth faceting effects were observed with increasing source temperature.

Fig 5.34 shows the morphology of a representative sample with CdTe nanowires grown on a glass substrate. Prior to the nanowire growth 5 nm of bismuth were thermally evaporated on the glass substrate. The nanowires were grown after 5 mins of CdTe growth at $T_{src} = 490^\circ\text{C}$, $T_{sub} = \sim 410^\circ\text{C}$ (substrate heater off) under 10 Torr (50 sccm

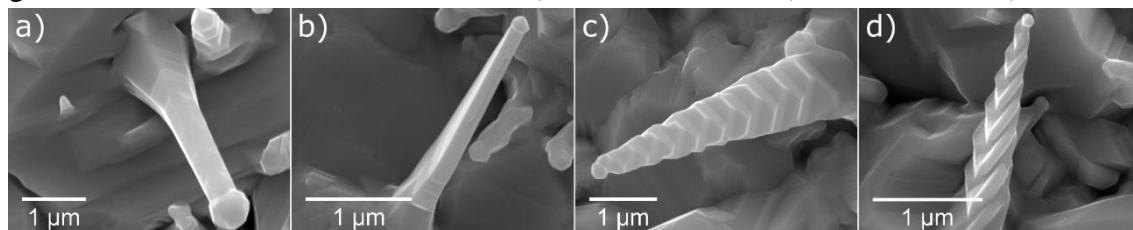


Fig. 5.33 Various morphologies of the Bi-catalysed CdTe nanowires: nanowires with hexagonal (a) and rectangular (b) cross-sections. Nanowires with sidewalls that exhibited periodic sawtooth faceting (c, d).

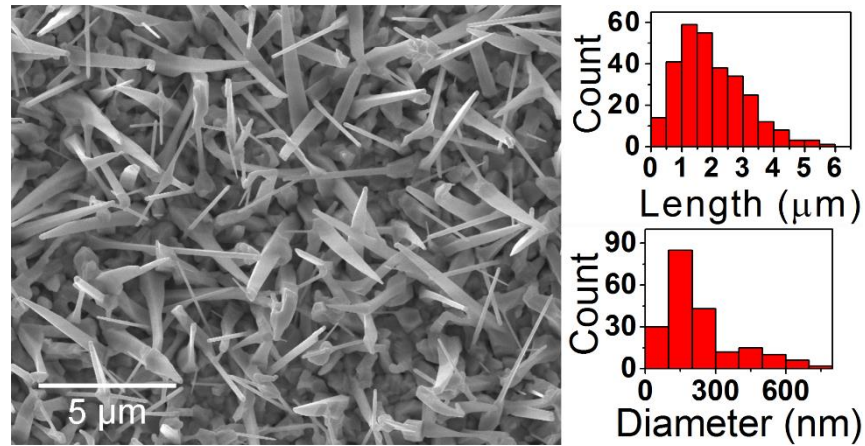


Fig. 5.34 Secondary electrons SEM image of Bi-catalysed CdTe NWs. A 5 nm thick Bi film was deposited on a glass substrate and CdTe growth was carried out at $T_{src} = 490^{\circ}\text{C}$, $T_{sub} = \sim 410^{\circ}\text{C}$ (substrate heater off), 10 Torr, 50 sccm H_2 , 5 mins without any annealing step. Histograms of the nanowires length and diameter, obtained by analysing ~ 200 nanowires are shown on the right. The diameters of tapered nanowire

H_2). The NW growth process did not include any annealing. The dimensions of ~ 200 nanowires were analysed from field of view SEM micrographs (the diameters were measured close to the bottom of the nanowires) and the average nanowire length was $2 \pm 1.1 \mu\text{m}$ and the average diameter $226 \pm 153 \text{ nm}$. Faceted-spherical particles were observed at the tips of most of the nanowires. High-magnification secondary and back-scattered electron images of an individual nanowire are shown in Fig 5.35 with the bright droplet assumed to be the Bi catalyst (confirmed using SEM/EDX analysis). The distribution of the nanowires length and diameter and catalysts size were obtained by analysing ~ 200 nanowires. Although a clear relation could not be established, tapered

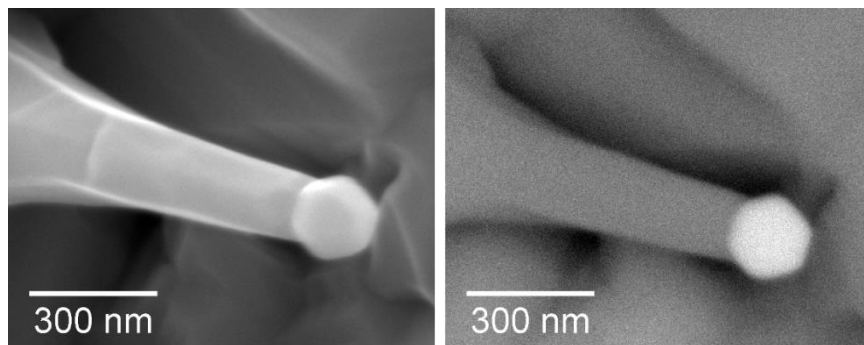


Fig. 5.35 Secondary (left) and back-scattered (left) electron SEM images of an individual Bi-catalysed CdTe nanowire

and thicker nanowires were longer than the straight and thin. The average nanowire density was $\sim 10^7 \text{ cm}^{-2}$, which is at least two orders of magnitude lower than the average density of the Bi nanoparticles.

The elemental compositions of a typical nanowire's trunk and tip were determined using SEM/EDX elemental analysis. Data were collected from six points with varied distance from the centre of the catalyst (Table 5.10) and the Cd, Te and Bi content was plotted against the distance (Fig 5.36). The electron beam energy used in the measurement was 15 keV and a maximum electron penetration depth of $\sim 600 \text{ nm}$ in Bi and $\sim 700 \text{ nm}$ in CdTe was calculated using the Casino Monte Carlo simulation software²⁸. Therefore, the point measurements both at the nanowire's trunk and tip probably include instrumental errors up to a certain extent. The mean values of the Cd, Te and Bi content at the droplet (0, 60 and 120 nm data points) were $40 \pm 1 \text{ at.}\%$, $36 \pm 2 \text{ at.}\%$ and $23 \pm 1 \text{ at.}\%$ respectively. This confirms the hypothesis that such droplets at the nanowire tips are the remaining Bi catalysts. A fast decrease of the Bi content was observed with

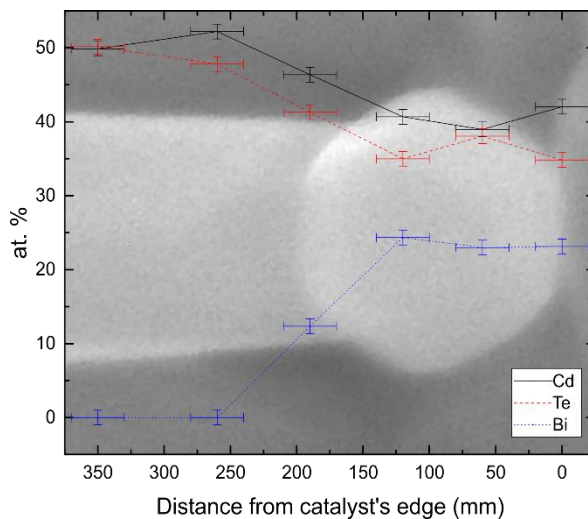


Table 5.10 Cd, Te and Bi content for varying distances from the centre of the Bi droplet.

Distance from catalyst's edge (nm)	Cd (at.%)	Te (at.%)	Bi (at.%)
0	42	35	23
60	39	38	23
120	41	35	24
190	46	42	12
260	52	48	0
350	50	50	0

Fig. 5.36 Plot of the Cd, Te and Bi atomic content in the trunk and tip of an individual Bi-catalysed CdTe nanowire. Background: secondary electron SEM image of the measured CdTe nanowire. $E_{beam} = 15 \text{ keV}$; the penetration range in Bi is $< 600 \text{ nm}$ and in CdTe $< 700 \text{ nm}$.

increasing distance. At ~ 60 nm from the nanowire trunk-droplet interface (260 nm from the catalyst's edge), the Bi content dropped to zero.

5.5.4 Discussion of the Bi-catalysed growth of nanowires

5.5.4.1 The effect of H_2 on the de-wetting of Bi thin films

As shown in Section 5.5.1.1, the de-wetting of Bi thin films and the formation of catalyst droplets by annealing in N_2 ambient was difficult to achieve. It was speculated that this was due the fast formation of oxide layers on the surface of the Bi films during or after the Bi deposition and the annealing process. Indeed, Kim *et al*⁷⁰, have shown that annealing of sputtered Bi films at temperatures greater than 250°C led to the formation of bismuth oxides, although the annealing was carried out in hydrogen atmosphere. Additionally, according to Leontie *et al*⁷¹, amorphous bismuth oxide layers can form up at the substrate – film interface during the thermal oxidation of Bi films on glass substrates. This sandwich structure may prevent the solid state de-wetting by passivating the film and enhancing its overall stability, which in turn blocks the surface diffusion and void nucleation. This is in accordance with Hieke *et al*⁷² and their findings on the solid state de-wetting of Al thin films. Although bismuth oxide is stable at the annealing temperatures used – it has a melting point of 860°C – metallic Bi that may exist beneath the oxide layers can, theoretically, diffuse outside and lead to the formation of nanodot arrays by liquid state de-wetting. However, this would require a reducing or at least inert atmosphere in order for further oxidation to be prevented. Indeed, Niu *et al*⁷³ have demonstrated the formation of bismuth hollow nanospheres by growing a thin bismuth oxide layer on the nanospheres surface via annealing at 180°C in an oxidising ambient. The authors have shown with *in situ* TEM measurements that metallic Bi diffuses out of the oxide shell, converts to bismuth oxide until the core is fully depleted. Thus, the smearing of the surface morphology that was observed at

500°C can be ascribed to further oxidation of the bismuth films due to the absence of a reducing atmosphere.

The de-wetting of bismuth thin films and the formation of Bi nanodots was achieved by introducing a H₂ flow in the CSS reactor during the annealing process. Chernogorenko *et al*⁷⁴ have shown that the reduction of Bi₂O₃ to metallic Bi can take place during the annealing of bismuth oxide films in a molecular/atomic H₂ stream. According to the authors, hydrogen diffuses and chemically reacts with the surface oxide yielding pure bismuth. This is in accordance with other reports^{75,76} on the reduction of oxides by annealing in a H₂ atmosphere. Therefore, in this work it is postulated that H₂ acts as a reducing agent, which reduces the bismuth oxides to metallic bismuth and prevents reoxidation of the latter. The discrepancy between this work and the findings of Kim *et al*⁷⁰ on the reduction of bismuth oxides in hydrogen atmosphere can be ascribed to the differences in the experimental setups.

5.5.4.2 Development of Bi nanodot arrays in H₂ ambient

Bi nanodots were fabricated on CdTe-coated and bare glass substrates, Mo foils and Si wafers. Bismuth has a melting point of 271°C and forms eutectic points with all used substrates at the annealing temperatures in this work. Therefore, since oxidation phenomena were impeded by using a H₂ ambient, the generation of the nanodot arrays was ascribed to the liquid state de-wetting of the Bi films.

Increasing annealing temperatures resulted in less dense arrays with larger nanodots in a similar way to the development of Au nanodots (5.4.5.1). Additionally, bismuth evaporation or reaction during the annealing process is another factor that may influence the nanodot density resulting in less dense arrays at higher temperatures.

5.5.4.3 Growth mechanism of CdTe nanowires fabricated in N_2 ambient

As shown in Section 5.5.2, CdTe growth on Bi coated glass substrates in N_2 atmosphere resulted in the formation of CdTe nanowires with random cross-sections, diameters and lengths. Here, the growth mechanism of these structures is investigated.

Although the use of Bi was essential, since no nanowires was observed in Bi-free samples, Bi-catalysed VLS or VSS methods were ruled out. One indication supporting this is the total absence of catalyst droplets at the tips of the nanowires. Although catalysts during the VSS or VLS nanowire growth may shrink or even disappear due to diffusion, incorporation, evaporation or reaction phenomena^{3,59}, in most of the cases droplets can be seen at the tips of the nanowires especially during the initial growth stages. Moreover, in Section 5.5.4.1, it was speculated that the unsuccessful break up of Bi films and formation of nanodots by annealing in N_2 atmosphere was due to oxidation phenomena. The presence of surface oxides on the Bi catalysts can act as a diffusion barrier and prevent the supersaturation of the catalysts with Cd and Te adatoms. This is in accordance with reports on the use of Al in the VLS growth of Si nanowires⁷⁷. Therefore, a bismuth-induced vapour-solid growth mechanism is postulated, which initially favours the columnar growth of CdTe islands over the formation of a CdTe complete film. At longer deposition times though, either lateral growth and coalescence of the nanowires or the overgrowth of a two-dimensional CdTe thin film on top of the nanowires becomes dominant. Nevertheless, additional investigations are required for a more detailed understanding of the growth mechanism.

5.5.4.4 Growth mechanism of CdTe nanowires fabricated in H_2 ambient

Morphological studies of CdTe nanowires grown in H_2 ambient revealed a wide range of nanowire geometries with catalysts at the tips indicating a VLS or VSS growth mode. Yet, determining which of the two modes was dominant during growth was difficult.

Firstly, the growth temperatures used in this work (400°C – 490°C) are in good agreement with findings reported elsewhere^{78–81} on the Bi-catalysed VLS growth of CdTe nanowires. On the contrary, the highly-faceted surface of the catalysts along with the high density of crystalline defects that was observed in some nanowires suggest that a VSS growth mode took place. Moreover, SEM/EDX microanalysis showed a high concentration of impurities in the spherical droplet, which is indicative of VSS grown nanowires⁴⁸, while in VLS a pure metal catalyst is expected^{49,50}. According to Di Carlo⁵⁴ an increase of the melting point of the ternary Au – Cd – Te during the growth of Au-catalysed CdTe nanowires may occur with increasing Cd concentrations, which may shift the growth mechanism from VLS to VSS. Similar implications may exist in the Bi – Cd – Te system, but have not been investigated. Thus, it is speculated that, in this work, both VSS and VLS growth modes led to the generation of CdTe nanowires.

The early stages of the growth mechanism for the nanowires generated in this work are now discussed. Firstly, it is postulated that at the growth temperatures the Bi catalysts are in the liquid state as discussed in Section 5.5.4.1. According to the Bi – Cd⁸², Bi – Te⁸³ and Bi – CdTe⁸⁴ phase diagrams, liquid solutions of all three binary systems coexist at the growth temperatures. However, due to the complexity of the system, it is unclear whether Cd and Te atoms diffuse directly into pure Bi or into Bi – Te alloyed catalysts, supersaturate them and precipitate as CdTe. Nevertheless, the VLS growth of the nanowires is more likely to be Bi/Te-catalysed, since bismuth is known to be highly volatile and, at the growth conditions used in this work, the formation of a Bi – Te alloy would enhance the catalyst stability. This is in accordance with the findings of Refs. ^{78,85–87}. For the case of Bi-induced VSS growth of CdTe nanowires, the catalysts are required to be in the solid state during the growth process, which can only be achieved with the formation of a Bi_xTe_y compound. Yet again, a model describing the growth

mechanism in detail could not be inferred due to the complexity of the system. Overall, for a further understanding of the growth mechanisms, *in situ* elemental microanalysis using HRTEM/EDX and investigation of the Bi – Cd – Te ternary alloy is required, which was not included in this work.

5.5.4.5 Morphology of CdTe nanowires fabricated in H_2 ambient

Here, the various morphological features of the obtained nanowires are discussed. As expected, the growth variables, such as source temperature, gas pressure and ambient and deposition time proved to be crucial for the nanowire properties, but optimal values for the fabrication of NW arrays were not reached due to the irreproducibility.

Nanowire density: The average NW density was in the range of $\sim 10^7 \text{ cm}^{-2}$, which is at much lower than that of the Bi nanodot arrays. As postulated in Section 5.5.4.4, for VLS/VSS growth to occur, it is likely that the formation of liquid or solid Bi – Te catalysts is required. Therefore, it is highly probable that the growth of a thin CdTe film precedes the nanowire growth which may result in the burial of the catalyst nanodots up to some extent. Moreover, as shown in Section 5.5.1.2, the breadth of the diameter distribution of the Au nanodots can be greater than 100 nm. Thus, since NW growth proceeds upon the saturation of the catalysts with the semiconductor material, the growth rate is expected to decrease with catalyst size and even terminate above certain diameters.

An additional factor that can result to lower nanowire densities (and other effects as discussed below) is the high volatility of bismuth. An indication of this, is the fact that a significant amount of nanowires did not bare any catalyst droplets at their tips. More specifically, the substrate temperature regime that led to nanowire structures was found to span between 400°C and 490°C, a temperature regime that bismuth is prone to

evaporation. Possibly, lower substrate temperatures and higher pressures could minimise the bismuth evaporation rate, but this was not possible. In the employed CSS reactor, the source and substrate temperatures are coupled with a maximum temperature difference of $\sim 70^{\circ}\text{C}$, because of the short distance that separates the source tray and the sample stage. Therefore, since a source temperature of at least 470°C was required for the sublimation of CdTe, the minimum achievable substrate temperature was $\sim 400^{\circ}\text{C}$. Although higher deposition pressures did reduce the evaporation rate of Bi, NW growth was not possible. This was because the number and frequency of inter-atomic collisions increase with pressure and, thus, the arrival rate of Cd and Te adatoms to the sample's surface decreases. Therefore, the in-diffusion of Cd and Te atoms to the catalysts becomes lower than the out-diffusion and supersaturation of the catalyst was not possible.

Catalyst losses become more intense with the application of H_2 as oxide reducing agent either due to formation of volatile bismuth hydrides, as in the hydrogen transport vapour growth method^{88,89} or due to higher heat conductance.. This can affect the supersaturation of the catalysts with Cd and Te adatoms and the overall nanowire growth mechanism. Moreover, H_2Te can react with the sublimated Cd atoms according to $\text{Cd} + \text{H}_2\text{Te} \rightarrow \text{CdTe}$, which may favour the formation of CdTe layers and suppress the NW growth. Yu *et al*⁹⁰ have shown that Bi droplets at the tips of Si NWs can be completely removed by exposing the nanowires to a H_2 plasma treatment. This was ascribed to the high volatility of Bi and the formation of bismuth hydrides. Finally, other factors that may influence the nanowire density is catalyst coalescence, migration or incorporation at the nanowire growth temperatures.

Nanowire tapering: The nanowire arrays that were generated comprised straight and tapered nanowires. In general, tapering effects in nanowires grown by the VLS method occur due to instability and gradual volume reduction of the catalyst through diffusion, incorporation, evaporation or reaction phenomena^{3,59} and the uncatalysed vapour – solid growth on the nanowire sidewalls^{56,60}. As discussed above, the volatility of bismuth and the formation bismuth hydrides can lead to significant catalyst losses and tapering effects in turn. Lateral growth due to the uncatalysed vapour – solid growth on the nanowire sidewalls increased with nanowire length, since for longer nanowires the diffusion length of the Cd and Te adatoms becomes smaller than the nanowire length.

Nanowire cross-sections: Nanowires with rectangular and hexagonal cross-sections (*rectangular* and *hexagonal* nanowires) and random growth directions were observed. For a detailed understanding of the reasons for the two cross-section types TEM crystallographic investigations are required, which were not included in this work. Nevertheless, a very detailed investigation of similar findings has been reported by Williams⁵¹. Williams have analysed Au-catalysed VLS grown CdTe nanowires using TEM and found that they adopted both rectangular and hexagonal cross-section. Fast Fourier transformations showed that the growth axis of the hexagonal nanowires was the $\langle 111 \rangle$, while that of the rectangular nanowires was the $\langle 112 \rangle$. Williams explained the different geometries using Wulff constructions, which predict the equilibrium shape of a crystal based on energy minimisation arguments. Thus, in the case of hexagonal nanowires with $\langle 111 \rangle$ growth axis the sidewalls are formed by six $\{110\}$ facets, while rectangular nanowires with $\langle 112 \rangle$ growth axis have two $\{111\}$ and two $\{110\}$ facets. For a general review about the factors that affect NW growth direction and the properties of the different geometries, the reader is referred to Ref. ⁹¹

Sidewall sawtooth faceting: Nanowires with sidewalls depicting sawtooth faceting have been previously reported in the VLS growth of Au-catalysed Si^{92,93}. Schwarz *et al*⁹² have ascribed the sawtooth effects on Si nanowires to surface energy variations of the sidewall facets. Specifically, their simulations predicted that sawtooth faceting can be controlled by changing the energies of the {111} and {113} facets during growth. This was experimentally validated by introducing and adjusting accordingly an O₂ flow, which presumably had a direct impact on the facets energy. Moreover, they have demonstrated that tapering effects are, often, observed in nanowires depicting sawtooth faceting because of a gradual Au loss. A different sawtooth structure has been observed in III – V nanowires, i.e. GaAs⁹⁴, InP⁹⁵ and InAs⁹⁶. Algra *et al*⁹⁵ have ascribed the sawtooth faceting in InP nanowires to the formation of twinning superlattices. Although InP is commonly found in the wurtzite crystal structures, zincblende InP nanowires with periodic twinning superlattices were fabricated by tuning the nanowire diameter and Zn concentration. A model based on the evolution of the nanowire cross-section during growth and the induced distortion of the catalyst droplet was proposed in order to explain the periodic twinning. This is in accordance with Caroff *et al*⁹⁶ that have ascribed sawtooth faceting in InAs nanowires to the formation of polytypic and twinning superlattices. Bulk CdTe, usually, crystallises in the more stable zincblende symmetry. However, since the zincblende and wurtzite phases have similar energies, structures with both phases have been reported⁹⁷. Although wurtzite CdTe is less stable than the zincblende in the bulk⁹⁸, the additional degree of freedom in nanowire growth can lead to the growth of wurtzite CdTe nanowires. Indeed, Luo *et al*⁹⁹ have demonstrated the growth of both wurtzite and zincblende CdTe nanowires by regulating the growth parameters of their sputtering deposition method. Moreover, Williams *et al*¹⁰ have demonstrated the existence of extended defects, such as stacking faults, polytypes

and twins in Au-catalysed CdTe nanowires, which occasionally exhibited a periodicity without the occurrence of sawtooth faceting though. Therefore, it is speculated that the sawtooth faceting observed in this work is more likely due to polytypic and twinning effects.

5.6 Conclusions

In this chapter, the catalyst-free template-assisted and catalysed VLS growth of CdTe nanowires were investigated. While the template-assisted growth experiments did not yield any nanowire growth, the VLS growth of CdTe nanowires using the Au and Bi catalysts was successfully demonstrated.

In Section 5.2, two different template types were explored: holey templates exhibiting a random distribution of pinholes and patterned antidot templates film developed with the nanosphere lithography technique. While the development of holey templates could not be verified with certainty, the fabrication of a wide range of antidot templates was successful. Antidot arrays with well-defined pores and large close-packed ordered domains were generated on glass substrates, while arrays developed on CdTe-coated substrates were less ordered and had pores with fuzzy boundaries. It was speculated that the morphological differences between templates grown on bare and CdTe-coated substrates were due to surface chemistry effects and variations in the spheres-substrate interactions. Therefore, a further optimisation of the spin-coating process is required for the development of templates on CdTe-coated substrates in order to achieve a higher density of ordered antidot arrays.

CdTe growth on holey and antidot templates resulted in the conformal coating of the surface and no nanowire growth was observed. Selective area growth starts with the preferential nucleation of the adatoms at the pores' corners and nanowire growth is

promoted due to surface energy anisotropy or preferred epitaxial growth of certain crystal facets. Thus, the geometry of the pores and the surface properties of the templates and the exposed substrate is of great importance. In this work, a) the absence of an underlying CdTe buffer layer in templates developed on bare glass substrates and b) the fuzzy geometry of the pores in the case of templates developed on CdTe-coated substrates were the limiting factors preventing nanowire growth. In addition to this, the CdTe selective nucleation in the pores was further limited by the oxidation of the underlying CdTe surface, which was confirmed by SEM/EDX elemental analysis. Overall, CdTe NW growth using holey and antidot templates was unsuccessful and requires further investigations. However, the development of antidot templates using NSL offers good control over the geometry of the pore array and, with further optimisation, they can be potentially used for the selective area growth of nanowires for PV applications. Ideally, this would require templates with a high density of pores and abrupt sidewalls on oxide-free CdTe substrates. On the contrary, the use of holey templates offers very little control over the geometrical characteristics of the pores. CdTe nanowires grown by this method, usually, have very low densities and diameters of some tens of nanometres, making them unsuitable for PV applications.

The generation of catalyst arrays made of Au and Bi was explored and the catalyst-assisted VLS growth of CdTe nanowires was tested. Au nanodot arrays were successfully generated on Si wafers and bare or CdTe-coated Mo foils by annealing at the 300-500°C temperature range (Section 5.4). Since the correlation between the Au layer thickness and the mean interparticle distance and particle diameter did not satisfy the linear hydrodynamic spinodal de-wetting theory requirements, a solid state de-wetting process was speculated, which agrees with the low annealing temperatures. The

annealing temperature, pressure, time, the Au layer thickness and the substrate properties were found to influence the size and the density of the nanodot arrays.

Straight and tapered randomly aligned Au-catalysed nanowires with average diameters from 100 to 500 nm and lengths up to 10 μm were successfully fabricated by CdTe CSS. Au droplets were observed at the nanowire tips, which is a hint of the VLS growth mode. This indication is further amplified by the fact that the catalysts have a spherical shape with diameters significantly larger than that of the nanowire trunk at the catalyst-nanowire interface. Lastly, the growth conditions used in this work were very similar to other reports on the VLS growth of Au-catalysed CdTe nanowires by CdTe CSS. Conclusively, it was speculated that the nanowire growth proceeded via a VLS mode. The nanowire tapering was ascribed to vapour-solid deposition on the nanowire sidewalls due to low diffusion lengths, since higher degree of tapering was observed in longer nanowires. Apart from nanowires, the growth of worm-like structures with droplets larger than those at the nanowire tips was observed. This was ascribed to a combination of slow supersaturation and an interplay between the VLS and VSS growth mechanisms that occur in larger catalysts.

Finally, the effect of Au film thickness, deposition time, pressure and substrate temperature on the growth of Au-catalysed CdTe nanowires was demonstrated. Regardless the deposition conditions, the NW and NW-catalyst diameters decreased with Au film thickness, while the density and the catalysts at the tips of the worm-like nanostructures always increased with film thickness. This was ascribed to the number of big particles increasing on the expense of small with increasing Au film thickness. The deposition time dependence of NW growth was also studied with longer CdTe deposition times resulting in lower nanowire densities, thicker, longer nanowires and

more intense tapering effects. This is consistent with the VLS growth mode. Evaluation of the effect of deposition pressure showed more dense, shorter and thinner nanowires at higher pressures. At high pressures, the vapour flux that diffuse in the catalysts is decreased, which in return results in decreased nanowire growth rate. Finally, arrays with lower NW densities, high aspect ratios and less tapering were generated at higher substrate temperatures due to a combination of lower vapour flux and surface diffusion related processes.

Next, in Section 5.5, the generation of Bi nanodot arrays and the growth of Bi-catalysed CdTe nanowires was demonstrated. First, the effect of H_2 on the generation of Bi nanodot arrays is demonstrated. Bi nanodots were generated on CdTe-coated and bare glass substrates, Mo foils and Si wafers, where the use of a H_2 atmosphere limited the oxidation of the Bi films and reduced the bismuth oxides to metallic bismuth. Since bismuth has a melting point of 271°C and forms eutectic points with all used substrates at the annealing temperatures, the generation of the nanodot arrays was ascribed to a liquid state de-wetting process. Moreover, particle analysis results were in good agreement with the linear hydrodynamic spinodal de-wetting theory. Increasing annealing temperatures resulted in less dense arrays with larger nanodots, while bismuth evaporation was also observed at elevated temperatures.

The growth of a series of Bi-induced CdTe nanostructures was demonstrated both in N_2 and H_2 atmospheres. A vapour-solid growth mechanism was postulated for the growth of CdTe nanowires in N_2 atmosphere, which initially favours the columnar growth of CdTe islands and at longer deposition times bulk growth becomes dominant. CdTe nanowires were successfully grown on glass substrates in H_2 ambient. Although the growth conditions are in good agreement with other reports on the Bi-catalysed VLS

growth of CdTe nanowires, the highly-faceted catalysts, high density of crystalline defects and high impurity concentration in the catalysts suggest that a VSS growth mode took place. Thus, an interplay between the VLS and VSS modes was speculated. However, optimal growth conditions for the fabrication of Bi-induced nanostructures were not reached due to Bi volatility during growth and irreproducibility issues.

Overall, while Au nanodot and Au-catalysed CdTe NW arrays were successfully fabricated, the controlled growth of CdTe NWs using other catalysts and methods was less successful. We have shown that a range of Bi-induced nanostructures was grown using CSS CdTe, but the growth process suffered from irreproducibility issues. Thus, only the Au-catalysed CdTe nanowires were suitable for the development of CdTe/CdS core-shell nanowire PV devices which is presented in Chapter 6.

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6 Planar and core/shell nanowire CdTe/CdS solar cells grown on molybdenum substrates

6.1 Introduction

In this chapter, the development and characterisation of planar and nanowire CdTe/CdS solar cells on Mo foils is reported and the two are compared.

The fabrication techniques for the development of planar and nanowire devices, the growth conditions and the experiments conducted are described in Section 6.2. Both nanowire and planar CdTe absorber layers were fabricated in the CSS reactor, while the CdS and ITO additional layers were deposited using RF magnetron sputtering. Both device types adopted the ‘substrate’ configuration, i.e. Mo/CdTe/CdS/ITO, as shown in Fig. 6.1. The conformal coating of the nanowires and the development of core-shell NW structures was confirmed by SEM.

In Section 6.3, the optical properties of CdTe NWs and planar films were investigated using optical spectroscopy comparative analyses with the nanowires exhibiting reduced

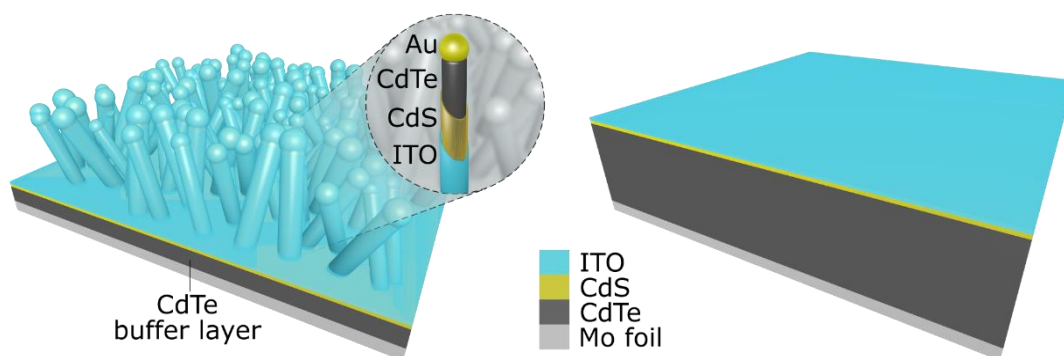


Fig. 6.1 Schematic diagrams of CdTe/CdS NW (left) and planar (right) solar cells.

optical losses. Next, in Section 6.4, results on the optimisation of a two-step Cl treatment and its effect on the PV performance of ‘substrate’ planar devices are presented. This resulted in planar devices with exceptional V_{OC} performance and conversion efficiencies of up to 8.52% and NW devices with lower efficiencies of up to 2.09%.

6.2 Experimental

6.2.1 Growth conditions

The growth conditions used for the deposition of the CdTe, CdS and ITO layers as well as the application of the $MgCl_2$ activation step are described below. The reader is referred to Section 5.4 for a detailed description of the development process and the morphological, chemical and structural properties of the employed Au-catalysed CdTe nanowires. Background information on the growth and characterisation methods and the characterisation techniques used can be found in Chapter 4.

Substrate preparation: Commercial Mo foils (Advent Research Materials Ltd, purity 99.95), 50 mm × 50 mm × 0.1 mm in size, were ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N_2 gun. To remove all surface

contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and DI water and dried with a N₂ gun again.

CdTe buffer layer deposition: The deposition of CdTe buffer layers of varied thickness was achieved by RF sputtering material off a 3" × 0.25", 99.99% pure CdTe target (PI-KEM Ltd). The growth conditions were as follows: 250°C substrate temperature, 100 W power, 10 mTorr Ar pressure, 60 mins. The thickness was measured at ~ 300 nm using profilometry.

CdTe absorber layer deposition: ~ 4 µm thick CdTe absorber layers were deposited in the CSS reactor using granular CdTe source (Alfa Aesar, 5N pure). Initially, the source was heated to 500°C under a static pressure of 300 Torr N₂ for 15 minutes. Next, the CdTe deposition was achieved by raising the source temperature to 605°C and by reducing the pressure to 60 Torr. After 30 minutes of deposition, the pressure controller was switched to 0 and then back to 300 Torr. This last step resulted in a high vapour flux of CdTe, which acted to reduce to the CdTe void density. Cooling to room temperature was achieved by rolling off the movable heaters with the samples in the reactor.

VLS growth of Au-catalysed NWs: CdTe nanowires were grown by CSS under conditions similar to those described in Section 5.4. 1.8 – 5.5 nm thick Au films were thermally evaporated on CdTe-coated and bare Mo foils and Au droplets were formed by annealing at 360°C for 30 mins under 300 Torr of N₂. VLS growth of NWs then followed at 570°C source temperature (T_{src}) and 530°C substrate temperature (T_{sub}) for between 5 and 20 mins under 20 – 40 Torr of N₂.

CdS window layer deposition: CdS layers were RF sputtered on planar and NW CdTe layers using CdS targets (3" × 0.25", 99.99% purity) from PI-KEM Ltd. The growth

conditions were: 150 W, 5 mTorr Ar pressure at 200°C for 36 minutes. The layer thickness was 130 nm thick, measured using profilometry.

ITO front contact layer deposition: 80 nm thick layers were RF sputtered using a In₂O₃:SnO₂ (90:10 wt.%, 99.99% pure, 2" × 0.25", PI-KEM Ltd) target. This was achieved at 350°C (substrate temperature), 2 mTorr Ar pressure for 2 hours. The average sheet resistance of the ITO layers was measured using the van der Pauw technique and was 17 Ω/□.

MgCl₂ treatment: Prior to the MgCl₂ treatment, the samples were cut to 25 mm × 25 mm sizes. The MgCl₂ treatment process¹ was employed and this is the first report of its application to substrate geometry CdTe/CdS solar cells. Prior to the chloride treatment, the samples were etched by submerging them in an N-P etching solution (70% H₃PO₄, 29% H₂O, 1% HNO₃) for ~ 10 secs followed by a DI water rinse. This has been demonstrated to enhance the incorporation of Cl and to increase the p-doping in the CdTe². Commercially available 1M aqueous MgCl₂ solution (Alfa Aesar) was spray-coated onto the etched surface of the planar and nanowire CdTe layers. Next, the samples were annealed in air at temperatures that ranged from 380 to 500°C for 15 – 30 mins inside the MgCl₂ tube furnace ('first' anneal). Following rinsing the samples were subjected to a second etching step before the growth the CdS and the ITO. Finally, the devices were completed with an optional final annealing step at 400 – 460°C for 15 – 30 mins in air inside the same tube furnace ('second' anneal).

6.2.2 Sample sets

Overall, ~ 80 samples were prepared and the PV performance of more than 200 solar cell contacts was measured for the purposes of this chapter. For the electrical characterisation (AM1.5 *J-V*, *EQE*) of the planar and NW solar cells, the samples were

mechanically scribed into individual rectangular cells, 0.04 cm^2 in size (Fig. 6.2). All samples were evaluated using AFM and SEM/EDX. Further specific detail is included below to define differences between the sample sets.

Optical properties of planar and nanowire CdTe layers (Section 6.3): In this section, a *planar* sample comprising a 200 nm thick sputtered CdTe buffer film on glass, a *NW* sample with Au-catalysed NWs grown on a similar CdTe buffer film and a *control* sample coated with the equivalent amount of CdTe to that used to make the full NW sample was employed as a control sample (Table 6.1). For the growth of the NWs, Au films with a graded thickness from 1.8 to 5.5 nm were used. The NW growth was carried out at $T_{src} = 570^\circ\text{C}$, $T_{sub} = 530^\circ\text{C}$, 20 Torr, 20 minutes. The NW arrays had an average density of 10^6 cm^{-2} , average lengths from 5 to 10 μm and average diameters from 400 to 900 nm. The transmittance and reflectance measurements were carried out using an integrating sphere in a Shimadzu SolidSpec-3700 spectrophotometer.

Optimisation of the MgCl_2 activation process of planar and NW ‘substrate’ CdTe/CdS on Mo foils (Section 6.4): For the purposes of this section, four planar CdTe/CdS solar cells that were finalised without the ‘second’ annealing step and another four identical cells that were finalised with the ‘second’ annealing step at 440°C for 30 mins were used. The ‘first’ annealing step was applied in all eight devices at 430°C for 15 mins.

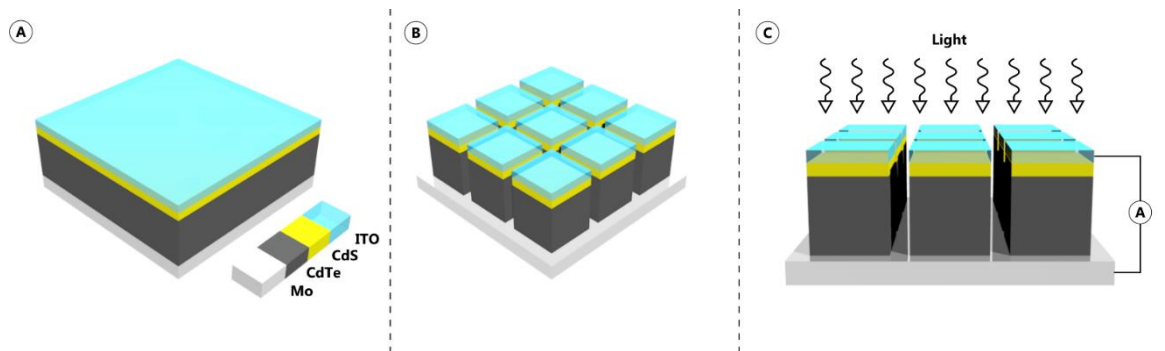


Fig. 6.2 Schematic diagram describing the scribing (A, B) and contacting (C) process of a planar Mo/CdTe/CdS/ITO ‘substrate’ cell.

Electrical characterisation of the highest efficiency planar and nanowire CdTe/CdS devices (Section 6.5): The highest efficiency planar CdTe/CdS device comprised a typical CdTe/CdS/ITO layer stack. For the highest-efficiency NW device, Au-catalysed NWs were grown on a $\sim 2 \mu\text{m}$ thick CdTe layer (CSS) using Au films with a graded thickness from 1.8 to 5.5 nm at $T_{src} = 570^\circ\text{C}$, $T_{sub} = 530^\circ\text{C}$, 20 Torr for 5 minutes. The NW arrays had an average density of $10^6 - 10^7 \text{ cm}^{-2}$, average lengths from 1.5 to 2.5 μm and average diameters from 220 to 320 nm. Both devices were grown on Mo foils and the ‘first’ annealing step was carried out at 430°C , 15 mins, while the ‘second’ at 440°C , 30 mins.

6.3 Optical properties of planar and nanowire CdTe layers

In this section, the optical properties of CdTe NWs and planar films grown on glass substrates are reported and compared.

The transmittance and reflectance curves of planar and nanowire CdTe layers grown on glass substrates are shown in Fig. 6.3. A third sample coated with the equivalent amount of CdTe to that used to make the full NW sample with an overall thickness of less than $1 \mu\text{m}$ was employed as a control sample. The configuration of the planar, nanowire and control samples are shown in Table 6.1. Evaluation of the reflectance curves showed significant reduction of the reflectance losses in the case of the NW sample. Specifically, incorporation of the Au-catalysed NWs reduced the reflectance of the planar sample from above 10% to below 1%. Slightly higher reflectance ($\sim 1\%$) was observed in the control sample. In additions to this, the NW sample had the lowest transmittance in both above- and below-gap regions with it being lower than 0.01% for wavelengths in the 300 – 750 nm range.

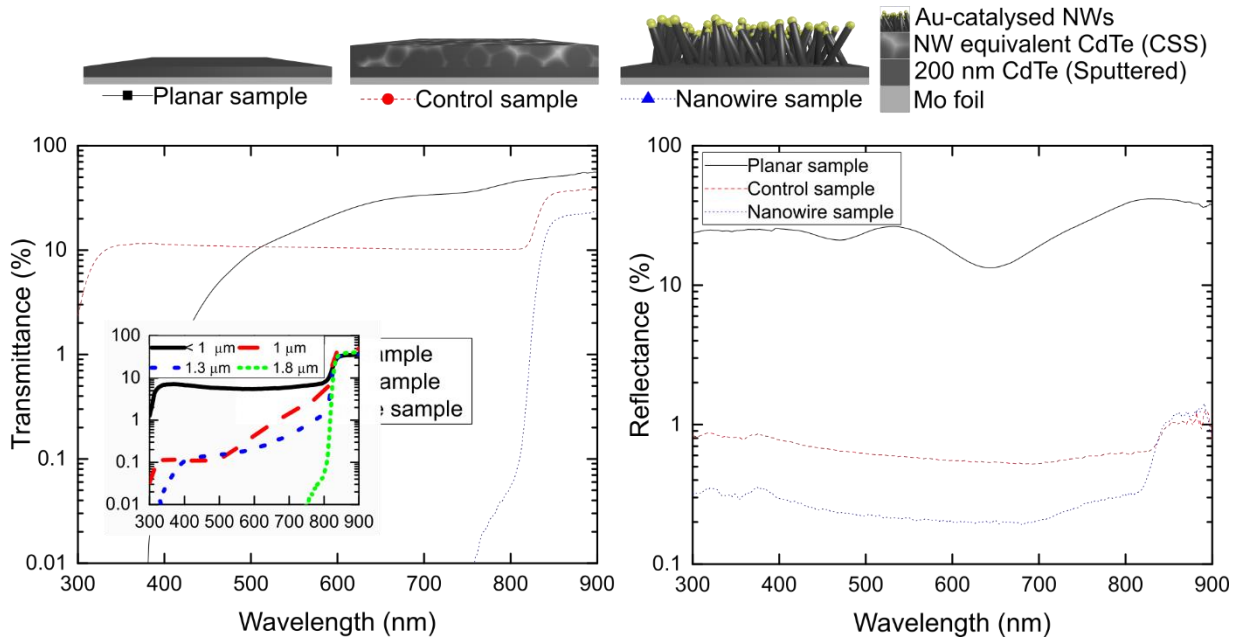


Fig. 6.3 Transmittance (left) and 5°- specular reflectance (right) log plots of planar and nanowire CdTe layers grown on glass substrates. The planar sample comprised a 200 nm thick sputtered CdTe thin film, while for the NW sample, Au-catalysed NWs were grown on a similar CdTe thin film. A third sample coated with the equivalent amount of CdTe to that used to make the full NW sample was employed as a control sample. The NW sample demonstrated significant reduction of the transmission and reflectance losses. Top: schematic diagrams of the three samples. Inset: transmittance curves of CSS-grown CdTe films of varied thickness.

While the NW and control samples demonstrated a distinctive transmittance drop around 820 nm (CdTe absorption edge), significant above-gap transmission was observed in the planar sample. Notably, although the planar sample has a thinner CdTe layer than the control sample, ~ 10% more light is transmitted in the < 500 nm spectral region. It was speculated that the enhanced transmittance is due to the formation of pinholes in the CdTe layer stack. In comparison to sputtered films which are usually more homogeneous, typical CSS-grown CdTe films exhibit pinholes penetrating partly or completely the layer. Moreover, due to recrystallisation and grain growth phenomena, which take place during the CSS deposition of the NW-equivalent layer, pinhole nucleation may also occur in the underlying sputtered CdTe thin film. This was tested by measuring the transmittance of CSS-grown CdTe films with varied

Table 6.1 Absorber layer specifications of the planar, NW and control samples. Tauc plots were used for the calculation of the bandgap energies for all three samples.

Sample	CdTe absorber layer	E_g (eV)
Planar	200 nm (planar)	-
Nanowire	200 nm (planar) + NWs	1.49 ± 0.03
Control	$< 1 \mu\text{m}$ (planar)	1.47 ± 0.03

thicknesses and the respective plots are shown in the inset of Fig. 6.3. The formation of pinholes was confirmed by optical microscopy and the pinhole density increased with decreasing thickness.

Tauc plots (Fig. 6.4) were used for the calculation of the CdTe bandgap in the three samples and is shown in Table 5.1. In the case of the NW and control samples, a distinct linear regime was observed and the calculated bandgap values were $E_{g, NW} = 1.49 \pm 0.02$ eV and $E_{g, control} = 1.47 \pm 0.04$ eV, which are in good agreement with CdTe bulk values.

Overall, the incorporation of the NWs acted to reduce the transmittance and reflectance losses of thin CdTe films, which indicates that they are effective in increasing the optical performance for PV applications. Nevertheless, evaluation of the optical properties of the control sample showed that the NW-induced enhancement lessens with increasing CdTe thickness. Particularly, the enhancement effects of the NWs in samples with > 1.8

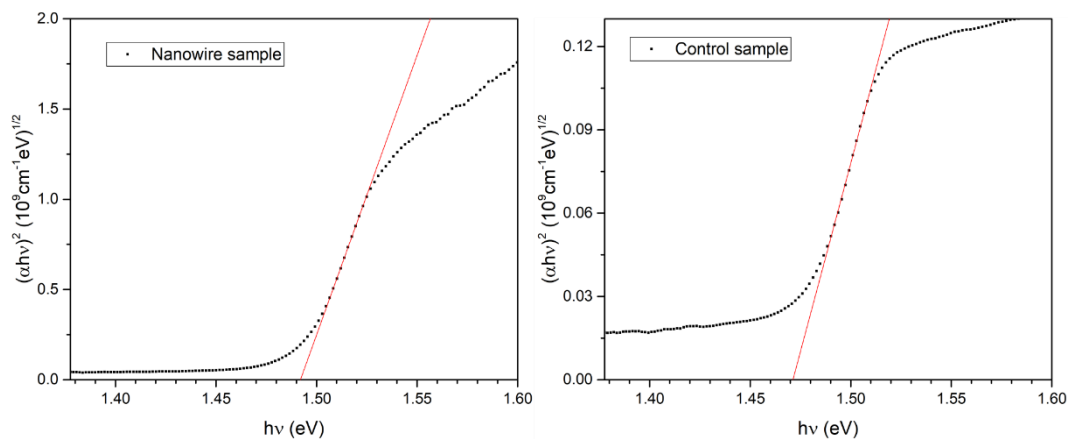


Fig. 6.4 Tauc plots for the nanowire (left) and control (samples) right. The CdTe optical band gap is determined from the x -intercept of the linear line fits (red lines).

μm thick CdTe layers becomes insignificant due to the optical absorption being already strong.

6.4 Optimisation of the MgCl_2 activation process of planar and NW ‘substrate’ CdTe/CdS on Mo foils

In this work, MgCl_2 was used instead of the widely-used CdCl_2 for the Cl activation process of the planar and NW CdTe/CdS devices. In addition to a ‘first’ annealing step after the CdTe deposition, it was found that a ‘second’ annealing step was required after the deposition of the ITO layer, in order to achieve the best performances in this work. Here, preliminary results on the effects of the MgCl_2 treatment and the post-growth final annealing step on the PV performance of ‘substrate’ planar and NW devices are presented.

Fig. 6.5a shows the effect of varying temperatures during the ‘first’ annealing step on the PV performance of planar devices. Although a slight performance increase was observed, compared to completely untreated samples (not shown here), all PV parameter values were very low with power conversion efficiencies below 1%. The same samples were annealed at 440°C for 30 minutes and the PV performance was

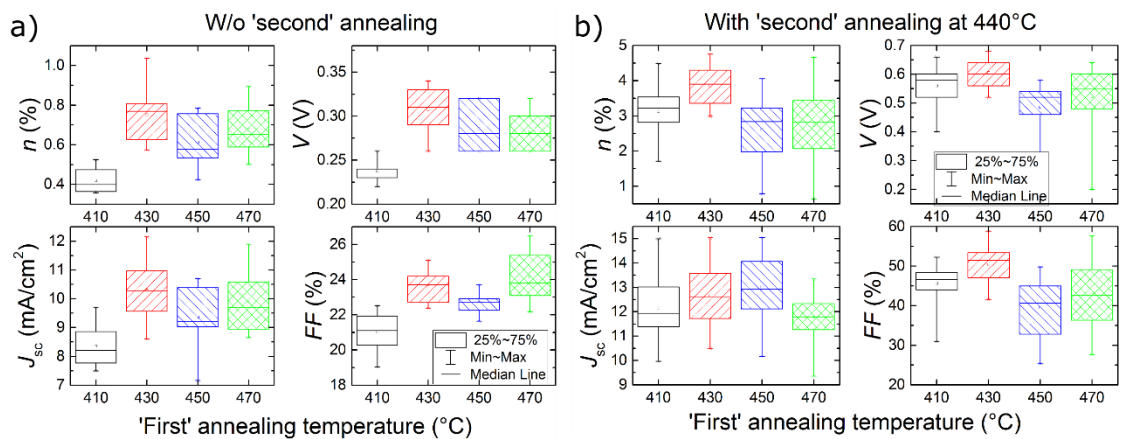


Fig. 6.5 Statistical analysis of the PV parameters η , V_{oc} , J_{sc} , FF for planar devices with (b) and without (a) the second annealing step and varying temperatures during the ‘first’ annealing step. Heating after the completion of the full device structure was essential to achieve the best performances in this work. $N > 26$ for each annealing temperature.

measured again (Fig. 6.5b). This resulted in significant enhancements in η , V_{OC} , J_{SC} and FF for all four samples. In these trials, the best performing device had $\eta = 4.75\%$, $V_{OC} = 0.6$ V, $J_{SC} = 12.34$ mA/cm² and $FF = 46.68\%$. Annealing at lower temperatures required increased longer annealing times while annealing at higher temperatures caused oxidation and thermal decomposition effects. In both cases, the PV performance of the samples decreased. A comparison of typical J - V and EQE curves of samples with and without the ‘second’ annealing step are shown in Fig. 6.6. As can be seen, the J - V curves demonstrated significant ‘rollover’ under high forward bias indicating an electron barrier at the CdTe-Mo contact. This is typical for CdTe solar cells especially in the ‘substrate’ configuration due to the high work function of CdTe (> 5.7 eV) that is higher than that of most metals. Evaluation of the EQE curves did not show any signs of a buried junction.

Similar performance trends were observed for NW devices (not shown here), but due to the lower efficiencies of the latter (Section 6.5), the effects of the two annealing steps on the PV performance were better visualised in planar devices.

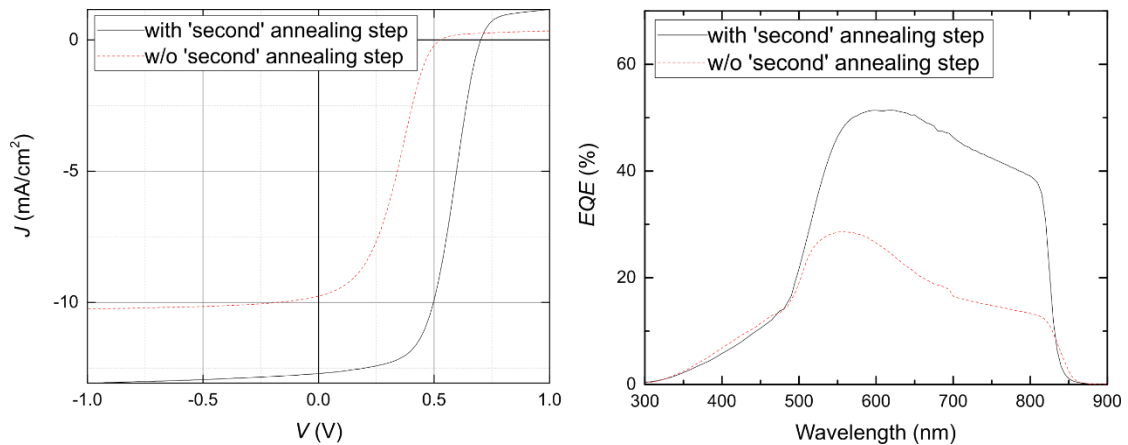


Fig. 6.6 Typical J - V (left) and EQE (right) curves of planar CdTe/CdS ‘substrate’ devices with and without the ‘second’ annealing.

Although a noticeable data spread was observed in the measured PV parameters and a temperature – performance relation could not be inferred with certainty, samples with a ‘first’ annealing at 430°C were generally superior to the rest of the samples.

6.5 Electrical characterisation of the highest efficiency planar and nanowire CdTe/CdS devices

In this section light and dark J - V and EQE , of the highest efficiency planar and NW CdTe/CdS devices in the ‘substrate’ configuration are presented. Both device types described in this section were optimised using the 2-step $MgCl_2$ activation route described in 6.4.

6.5.1 J - V

Fig. 6.7 shows the J - V curves of the best performing planar (a) and NW (b) devices under light and dark conditions. The performance parameters for the best planar and NW contacts as well as the average device values are shown in Table 6.2. Boxplots of the PV parameters for both device types are shown in Fig. 6.8. The series and shunt

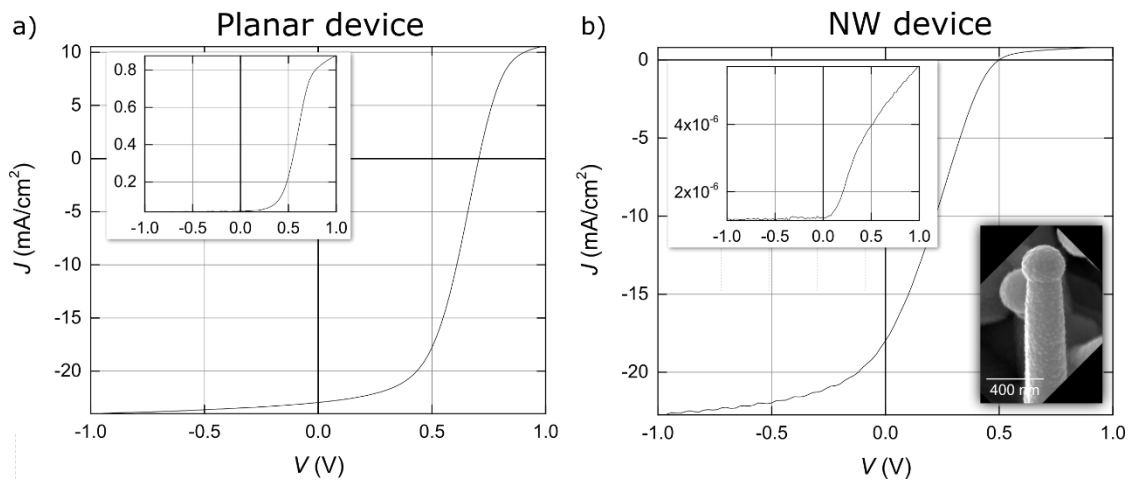


Fig. 6.7 J – V curves of the highest efficiency planar (a) and NW (b) cells under light and dark (insets) conditions. For the planar device: $\eta = 8.52\%$, $V_{OC} = 0.7$ V, $J_{SC} = 21.89$ mA/cm², $FF = 55.6\%$, while for the NW: $\eta = 2.09\%$, $V_{OC} = 0.5$ V, $J_{SC} = 17.05$ mA/cm², $FF = 24.47\%$. In both cases, severe ‘rollover’ was observed in the forward bias. Inset: SEM micrograph of a NW demonstrating the conformal coating with the CdS and ITO layers.

Table 6.2 Peak efficiency, R_S and R_{SH} values of the highest efficiency planar and NW CdTe/CdS devices.

Sample	Values	η (%)	V_{OC} (V)	J_{SC} (mA/cm ²)	FF (%)	R_S ($\Omega \cdot \text{cm}^2$)	R_{SH} ($\Omega \cdot \text{cm}^2$)
Planar	Max	8.52	0.7	21.89	55.6	9.6 ± 0.1	438 ± 16
	Avg	5.88 ± 1.53	0.68 ± 0.03	16.7 ± 3.5	51 ± 5		
NW	Max	2.09	0.5	17.05	24.47	96 ± 12	42.9 ± 2.2
	Avg	1.1 ± 0.4	0.36 ± 0.05	13.7 ± 3.5	22 ± 3		

resistances of the contacts were extracted from the inverse of the slope of the J - V curves near the V_{OC} and J_{SC} , respectively, and are shown in Table 6.2. While both devices demonstrated significant ‘rollover’ in the forward bias, which had a detrimental impact on the η , FF and R_S values, the effects were more pronounced in the case of the NW device. Another dominant performance limiting factor of the nanowire device is the poor R_{SH} values, which is indicative of shunting phenomena between the device’s layers. In accordance with this is the significant decrease in the V_{OC} maximum values from 740 to 460 mV. The PV performance of NW devices with varying NW dimensions was evaluated and compared, but a trend between performance and NW characteristics (density, length, diameter) could not be observed.

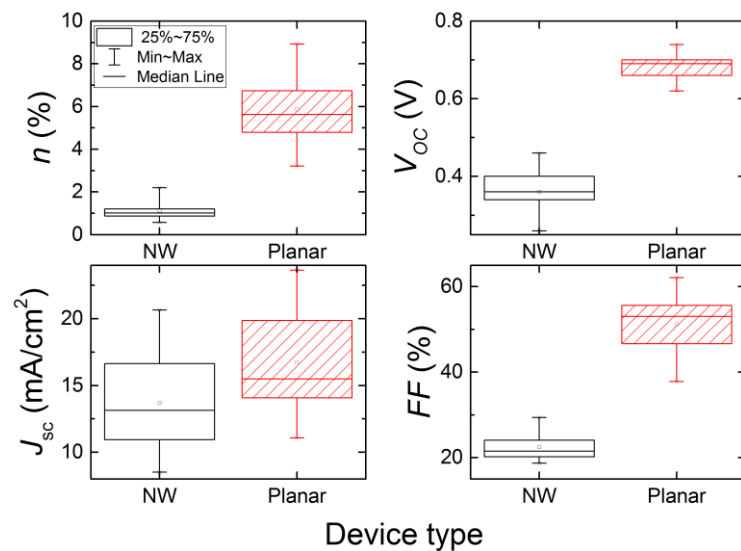


Fig. 6.8 Statistical analysis of the PV parameters η , V_{OC} , J_{SC} , FF for the highest efficiency NW and planar devices. $N_{NW} = 30$ and $N_{Planar} = 64$ for each device type.

6.5.2 EQE

Fig. 6.9 shows a comparison of *EQE* spectra of the highest efficiency nanowire and planar devices. Besides the $\sim 300 - 500$ nm region, where the NW device performs slightly better, the planar device had a significantly higher average *EQE* response overall. In order to investigate the *EQE* losses due to parasitic absorption, the spectra were divided in four spectral regions defined by the CdS, $\text{Cd}_x\text{S}_{1-x}$ and CdTe absorption edges. Additional *EQE* losses may occur due to reflections in the various interfaces of the device.

The *EQE* response of both devices was below 30% for wavelengths < 500 nm, i.e. for photon energies higher than the bandgap of CdS (2.42 eV). This is due to optical losses in the glass substrates, the ITO and the CdS layers. Although the parasitic absorption in the ITO layer can be negligible, since $E_{g, \text{ITO}} \sim 4$ eV, light absorption in the CdS layer is significant and undesirable, since it does not contribute to the current generation.

The absorption edge of CdS is at ~ 512 nm and due to its high absorption coefficient, an abrupt cut-off in the *EQE* response is expected. On the contrary, a more gradual slope

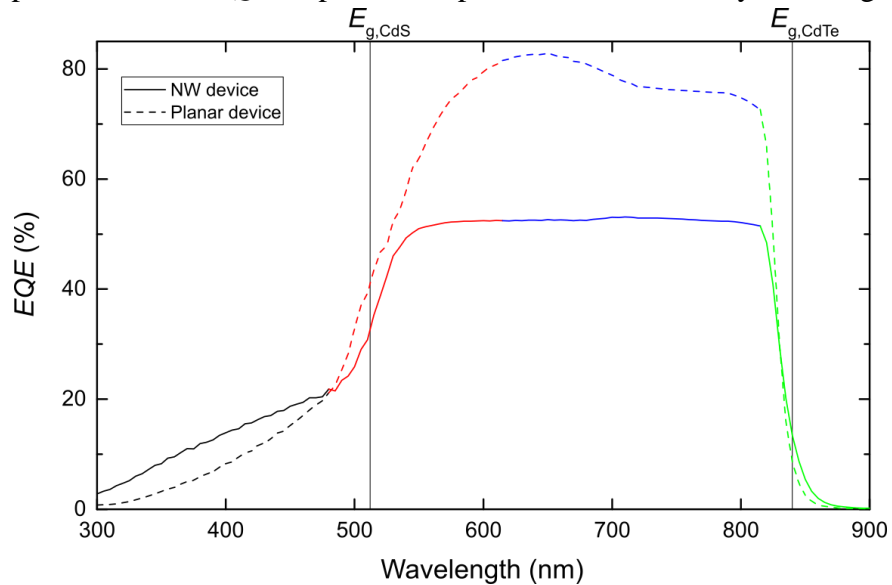


Fig. 6.9 *EQE* curves of the highest efficiency NW (solid line) and planar (dashed line) devices. The black, red, blue and green line segments represent the four spectral regions discussed in the text.

was observed in the $\sim 500 - 600$ nm spectral region. This is because of the intermixing effects between the CdS and CdTe layers which result in the formation of a $\text{CdS}_{1-x}\text{Te}_x$ alloyed layer³. The Te content in the intermixing layer lowers the bandgap energy of CdS creating a graded bandgap and shifting the p-n junction away from the metallurgical interface.

In the $\sim 600 - 800$ nm range, the *EQE* curve appears relatively flat with average values of $\sim 50\%$ for the NW device and greater than 70% (peaking at 83%) for the planar. While the *EQE* response of the NW device was almost constant in this region, small losses were observed in the spectrum of the planar device for wavelengths above ~ 650 nm. This can be ascribed to photons escaping the device without being absorbed⁴, photon – material interactions inside the device which can lower the photon kinetic energy below the bandgap energy of CdTe or low carrier mobility⁵.

Similar to the Te diffusion into the CdS layer, S diffuses into the CdTe layer to form a $\text{CdTe}_{1-y}\text{S}_y$ layer⁶. The layer intermixing degree lowers the CdTe bandgap and shifts the absorption edge to higher wavelengths affecting the *EQE* response for $\lambda > 800$.

The J_{SC} values of the planar and NW devices were calculated as follows: $J_{SC(\lambda)} = -q \int_{300\text{ nm}}^{900\text{ nm}} EQE_{(\lambda)} \Phi_{ph,\lambda}^{AM1.5} d\lambda$, where q is the elementary charge and $\Phi_{ph,\lambda}^{AM1.5}$ is the AM1.5 spectral photon flux⁷. The calculated values were compared to those extracted from the *J-V* curves (values in parentheses) and a significant discrepancy was observed: $J_{SC,PL} = 17.79$ (21.89) mA/cm^2 and $J_{SC,NW} = 12.78$ (17.05) mA/cm^2 . This was ascribed to errors in the solar simulator calibration, contact area measurement or the *EQE* measurement.

6.6 Discussion

6.6.1 Optimisation of the $MgCl_2$ process

Untreated planar and NW CdTe/CdS devices and devices without a ‘second’ annealing step demonstrated poor PV performance ($< 1\%$). On the contrary, devices that underwent a ‘second’ annealing step inside the $MgCl_2$ tube furnace after the deposition of the ITO layer had enhanced power conversion efficiencies.

Evaluation of the J - V and EQE curves (Fig. 6.5) for samples with and without a ‘second’ annealing step showed no evidence of a buried junction, but rather an overall enhancement of the junction quality was observed with significant increases in the V_{OC} , J_{SC} and FF values. Nevertheless, the sensitivity of the EQE measurements to junction position is limited by the minority carrier diffusion length and may not identify a shallow ‘buried’ junction if present. Therefore, it was speculated that during the ‘first’ annealing step, Cl diffusion, recrystallisation and grain growth effects resulted in grain boundary passivation and p-doping of the CdTe layer. However, optimal p-n junction quality and PV performance were only achieved after the ‘second’ annealing step. A similar two-step annealing process was used by Williams⁸ for the $CdCl_2$ treatment of ‘substrate’ CdTe/CdS solar cells. Using SIMS profiling, it was shown that a high temperature ($> 560^\circ\text{C}$) annealing step following CdS and ITO deposition was essential for optimal PV performance by promoting S, Te and Cl inter-diffusion. This is in accordance with the EQE response of single- and double-treated samples (Fig. 6.6) in the $\sim 500 - 600$ nm region: the gradual slope of double-treated samples is significantly longer, which is indicative of enhanced degree of $CdS_{1-x}Te_x$ intermixing. Although the ‘second’ annealing step in this work was performed at lower temperatures (440°C), the PV performance enhancement is likely to have happened because of similar effects. Despite the fact that $MgCl_2$ was not used directly during the ‘second’ annealing step,

Mg, Cl or MgCl_2 impurities that exist on the furnace surfaces are expected to evaporate during the high temperature treatment. This may further promote the inter-diffusion effects and lead to performance enhancements at lower annealing temperatures.

6.6.2 Performance losses in the NW devices

The core-shell CdTe/CdS nanowire devices presented in this chapter demonstrated significant PV performance losses with peak efficiencies of 2.09%. A comparison between the highest efficiency NW and planar devices showed considerable decline in all PV parameters for the NW device. One of the performance shortfalls was the lower V_{OC} value (0.5 V) of the NW device compared to that of the planar (0.7 V). This can be ascribed to a non-optimal CdS coating of the CdTe layer, i.e. the nanowires and the underlying buffer layer due to shadowing effects during the sputtering process. The very low R_{SH} value of $42.9 \Omega \cdot \text{cm}^2$ is in accordance with this and indicates a high density of shunting pathways. On the contrary, the shunt resistance of the planar device was one order of magnitude higher. Moreover, V_{OC} losses due to the pronounced ‘rollover’ effect should be taken in consideration, however further investigations using J - V - T measurements are required in order to measure and compare the back-contact barrier height. According to Williams⁹ the inclusion of a high resistivity transparent (HRT) ZnO layer between the CdS and ITO layers in similarly grown core-shell ITO/ZnO/CdS/CdTe nanowire solar cells act to reduce the electrical effect of shunting paths.

Another dominant performance limiting factor of the nanowire device is the low FF , which is both affected by the low R_{SH} and high R_S values. The high R_S values of the nanowire device $R_S = 96 \Omega \cdot \text{cm}^2$ compared to $R_S = 9.6 \Omega \cdot \text{cm}^2$ for the planar device, may

be ascribed to the higher back contact resistance because of the NW layer roughness or enhanced intrinsic resistance in the CdTe nanowires.

EQE spectra comparison between the nanowire and the planar devices showed a lower average *EQE* response for the nanowire device. A slightly higher efficiency was observed for low wavelengths, i.e. 300 – 500 nm, and it was attributed to lower optical losses in the CdS layer. Although the CdS layer deposition in both device types was carried out under the same sputtering conditions, variations in the thickness of the CdS layer are expected in the case of the NW device due to the anisotropic coating of the randomly oriented and dense nanowire arrays. Moreover, the spectral region of the gradual slope due to absorption in the $\text{CdS}_{1-x}\text{Te}_x$ intermixing layer appears shorter in the NW device. This indicates a lower degree of intermixing and can be attributed to a lower amount of diffused S into the CdTe layer. Furthermore, during the CdTe/CdS intermixing of thin CdS layers, complete consumption of the CdS layer can occur locally forming voids in the CdTe/CdS metallurgical interface. According to the Kirkendall effect¹⁰; in the case of asymmetric diffusion fluxes of S and Te atoms Te ($|J_S| > |J_{Te}|$) across the CdTe/CdS interface, the metallurgical interface may move inside the CdS layer leading to the thinning of the CdS. In the extreme case, that such a movement is not possible, voids may be formed. This in accordance with the observed low V_{OC} values and the speculated high density of shunting paths in the NW device. However, other phenomena may also contribute, such as enhanced stress relation in the crystal lattice of the nanowires¹¹, which can affect the CdS coating and the formation of the $\text{CdS}_{1-x}\text{Te}_x$ intermixing layer. In the ~ 500 – 800 nm range, the nanowire device *EQE* curve appears flat with average values of ~ 50% being much lower than that of the planar. According to the findings of Section 6.3, the optical transmittance and reflectance properties of both devices are expected to be very similar, which suggests

that the low *EQE* response of the NW device cannot correlate to optical losses or photons escaping the NW device.

In order to explain this discrepancy, the NW and buffer layer contributions to the overall PV performance of the NW device are now discussed. Devices with various NW length and diameter configurations were evaluated and of all those measured the highest performing NW device had the shortest nanowires. Furthermore, it is probable that the nanowires are fully depleted taking into consideration that the CdTe/CdS typical depletion region width is usually greater than 1 μm and that the NW diameters in this work were some hundreds of nanometres⁴. Therefore, since the buffer layer ($\sim 2 \mu\text{m}$) is expected to absorb more than 90% of the photons with energies greater than the CdTe bandgap, the presence of the NWs can be parasitical, i.e. light maybe absorbed by the nanowires but it does not contribute to the photocurrent. This could result from the absence of a *p-n* junction close to the peak position for carrier generation.

An additional factor that may had an adverse effect on the PV performance of the nanowire devices is the incorporation of impurities during growth. Although the findings of Williams¹² demonstrate a higher crystal quality in Au-catalysed CdTe nanowires than in polycrystalline CdTe films, it was speculated that Au introduced during the NW growth may introduce deep level defects. Such defects act as recombination centres for the photo-generated carriers with detrimental effects on the PV performance. Finally, due to the large surface-to-volume ratio, nanowire devices are likely to suffer from enhanced recombination through surface states¹³. Schmidt *et al*¹⁴, taking into consideration the effect of interface trap level density on the effective charge

⁴ Trials to grow thicker nanowires using larger Au catalysts led to worm-like nanostructures similar to those described in Section 5.4.

carrier density for thin nanowires, has derived an expression for a critical radius beyond which nanowires become fully depleted. In particular, unpassivated Si/SiO₂ nanowires with diameters of less than 300 nm and doping levels in the 10¹⁷ cm⁻³ regime are likely to be completely depleted by the surface states. This effect is expected to be even more evident in the case of a CdTe/CdS p-n junction due to the relatively low doping concentration of CdTe (> 10¹⁵ cm⁻³). Furthermore, Ford *et al*¹⁵ have shown that carrier mobility decreases with decreasing InAs nanowire diameters due to surface scattering effects. A series of experimental evidence^{16–18} has shown that such effects can be limited by employing surface passivation layers.

Overall, it was not possible to determine the main contribution to the generated photocurrent and distinguish between that of the nanowires or the underlying buffer layer. Thus, further investigation using *EBIC* measurements is required in order to evaluate the position of the photovoltaic junction and the nanowire performance.

6.6.3 Comparison of highest efficiency NW device to record efficiency CdTe NW-based devices

In this work, the development of core-shell CdTe/CdS NW photovoltaic devices with peak efficiencies of 2.09% has been presented. This performance comes second after Williams⁹ reported efficiency of 2.49%, which is the record device in this specific configuration and the parameters of the two are compared in Table 6.3. Although the η and V_{OC} are comparable, substantial differences can be observed in the J_{SC} and FF values. First, the discrepancies in the V_{OC} and FF values are being discussed. The enhanced V_{OC} in Williams' work can be ascribed to the inclusion of a ZnO HRT layer and a thicker CdS layer. Thicker CdS layers reduce the void formation in the CdS/CdTe metallurgical interface and improve the coating of the NW arrays, which decrease the shunting between the ITO and CdTe layers and the V_{OC} and FF losses. These effects

Table 6.3 Comparison of the record core-shell ITO/ZnO/CdS/CdTe nanowire solar cell to the highest efficiency cell of this work: CdTe (buffer), CdS and ZnO layer thickness, NW length (l) and diameter (d) average values, shunt, series resistances and PV performance parameters

	CdTe (μm)	CdS (nm)	ZnO (nm)	NW l/d ($\mu\text{m}/\text{nm}$)	R_{SH}/R_S ($\Omega.\text{cm}^2$)	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)
Ref. ⁹	1	200	20 – 40	5 – 10	269	2.5	523	13.9	34
				100 – 200	25.5				
This work	2	130	-	1.4 – 2.5	43	2.1	500	17.05	24
				140	96				

are further enhanced with the inclusion of the ZnO layer, which not only acts as a shunt blocking layer, but also can improve the junction quality by reducing the carrier recombination at the CdS/ITO interface¹⁹. Overall, this is in accordance with the lower R_{SH} values observed in Williams' work, which are associated with lower shunting effects. Finally, although the back-contact barrier height in this work was not measured, the higher R_S values (in this work) and a qualitative comparison of the J - V curves show a less pronounced 'rollover' effect in Williams' work. This had a beneficial impact on the V_{OC} and FF values.

Although the inclusion of ZnO HRT and thick CdS layers led to improved V_{OC} and FF values, current density shortfalls were observed. In particular, the significantly higher EQE losses in the blue spectral region (<500 nm), which are related to parasitical optical absorption in the CdS and the ZnO layers resulted in poor J_{SC} values. Furthermore, as in this work, it is highly probable that the NWs being 100 – 200 nm wide are fully depleted of charge carriers. Therefore, the combination of longer and thicker nanowires with a thinner underlying buffer layer is likely to result in lower carrier generation.

Zhang *et al*²⁰ have reported the development of a prototype core-shell nanostructured solar cell with a p-n CdTe-TiO₂ radial junction. This was accomplished by filling a

TiO₂ nanotube array with CdTe using pulsed laser deposition. However, due to the low estimated efficiency of $\sim 0.1\%$, a further comparison to the findings of this work could not be made.

6.6.4 Comparison of highest efficiency planar device to record efficiency ‘substrate’ CdTe/CdS devices

A comparison of the best cell in this work to the record efficiency ‘substrate’ CdTe/CdS devices is shown in Table 6.4. The up-to-date record devices have a highly-sophisticated configuration comprising a Mo/MoO_x/Te back-contact layer stack, a CdS bilayer, an i-ZnO HRT layer, a ZnO:Al front contact, Ni/Al front contact grid, MgF₂ anti-reflection coating, a double CdCl₂ activation treatment procedure and a finely adjusted Cu-doping process. This extremely complex fabrication process enabled peak efficiencies of 13.6% on borosilicate glass substrates and 11.5% on Mo foils. The authors suggest that the performance discrepancy is because of differences in the thermal mass of the two substrates and impurity diffusion from the foils. However, further PV performance losses may originate in the higher surface roughness of the Mo foils, which is typically tens to hundreds of nanometres. On the contrary, sputtered Mo layers on borosilicate glass substrates are expected to be very smooth owing to the low roughness of the glass substrates and the sputtering process, which typically produces

Table 6.4 Comparison of the record CdTe/CdS ‘substrate’ solar cells to the highest efficiency cell of this work

Ref	Comments	Substrate	η (%)	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)
22–26	Back-contact buffers + Cu doping + HRT layer + Ni/Al grid + MgF ₂ anti-reflection	BS glass/Mo	13.6	852	21.2	75.3
		Mo foil/Mo	11.5	821	22	63.9
8	ZnO HRT	Mo foil	8.01	690	22.4	51.9
This work	-	Mo foil	8.52	700	21.89	55.6

films of low surface roughness. This enables optimal film coverage of the subsequent layers, which can result in lower R_S and higher R_{SH} and, in turn, improved V_{OC} and FF values.

High efficiency CdTe/CdS solar cells suffer from ‘rollover’ effects under high forward bias due to the high work function of CdTe (> 5.7 eV) owing to its high electron affinity (~ 4.4 eV²¹). Although ‘rollover’ effects are typically observed both in the ‘superstrate’ and ‘substrate’ configurations, they are more pronounced in the latter. The inclusion of a MoO_x/Te buffer bilayer acted to reduce the effective barrier height, facilitating the formation of a quasi-ohmic back contact. This resulted in improved V_{OC} , FF and R_S values.

A first CdCl₂ treatment was applied after the CdTe layer in order to improve its properties and a second after the deposition of the first CdS layer. Although the latter was found to be beneficial for the optimal S, Te and Cl in- and inter-diffusion, it led to the formation of voids in the CdTe/CdS metallurgical interface. Therefore, a second CdS layer was used to eliminate potential shunting effects. This led to various cell performance improvements at the cost of a drop in the J_{SC} due to parasitical photon absorption.

As discussed in Section 6.6.3, the inclusion of ZnO HRT layers can lead to enhanced PV performance by limiting the shunting pathways between the CdTe and by reducing the carrier recombination at the CdS/front-contact interface. Lastly, the use of an anti-reflection coating increased the generated photocurrent due to reduced reflection losses and the Ni/Al grid improved the front-contact conductivity.

In this work, none of the above features were included in the development of the highest efficiency cell, which explains the relative decline in the η , V_{OC} and FF values. On the

contrary, the results in this work are in good agreement with similarly developed ‘substrate’ CdTe/CdS solar cells reported by Williams⁸. However, despite the inclusion of a ZnO HRT layer, Williams’ device had lower V_{OC} and FF values. This is probably due to the larger contact area of 0.0625 cm^2 used compared to the one in this work (0.04 cm^2) and other differences during the device fabrication process.

6.7 Conclusions

In this chapter, the fabrication and characterisation of planar and NW CdTe/CdS solar cell devices in the ‘substrate’ geometry was demonstrated.

First, spectrophotometry measurements of nanowires and thin-films demonstrated the superior optical properties of nanowire arrays compared to those of thin-films. Incorporation of Au-catalysed NWs on CdTe thin-films (200 nm) acted to reduce transmittance from above 10% to below 0.01% and reflectance from above 20% to below 1%. The enhancement effects of the NWs lessened with increasing CdTe thickness. This confirmed the effectiveness of NWs to absorb light and their suitability in the development of very thin devices, where the optical absorption is weak.

A preliminary study of the MgCl_2 activation process of planar and NW devices was performed using J - V and EQE measurements and was presented in Section 6.4. The results showed that optimal PV performance could only be achieved by using a two-step activation process, where a ‘second’ annealing step was applied after the deposition of the ITO layer. It was speculated that during the ‘first’ annealing step, after the application of MgCl_2 , grain boundary passivation and p -doping of the CdTe layer occurred, while optimal p - n junction quality and PV performance were only achieved after the ‘second’ annealing step.

Finally, in Section 6.5 the performance of planar and NW solar cell devices was evaluated and compared. Planar ‘substrate’-geometry solar cells were developed using the MgCl_2 alternative to CdCl_2 treatment with the best performing device having V_{OC} 700 mV, J_{SC} 21.89 mA/cm^2 , FF 55.6% and an efficiency of 8.52%. This was compared to the up-to-date ‘substrate’-geometry CdTe/CdS record device: a highly-sophisticated configuration with high-quality substrates, back-contact buffer layers, a CdS bilayer, improved doping and front contacts, HRT and antireflection layers and an efficiency of 13.6%. In this work, none of the above features were included in the development of the device. Thus, despite the current results being already very competitive, there are areas for further enhancements. The main efficiency limitations in this work were the relatively low V_{OC} and FF values, which were ascribed primarily to the back-contact barrier and shunting effects in the ITO/CdS/CdTe interfaces. Thus, the addition of ZnO HRT and back-contact buffer layers would enable higher V_{OC} and FF values and higher power conversion efficiencies.

Inclusion of Au-catalysed CdTe NWs always acted to reduce PV performance with the core-shell CdTe/CdS nanowire devices demonstrating significant performance losses and peak efficiencies of up to 2.09%. This performance comes second after the record device’s 2.49% in this specific configuration. The main performance shortfalls were the low V_{OC} (< 0.5 V) and R_{SH} ($< 50 \Omega\cdot\text{cm}^2$) values, which were ascribed to shunting between the ITO and the CdTe layers due to thickness variations and discontinuities in the CdS coating. This is in accordance with a slightly higher spectral response in the blue range for the NW devices, suggesting lower CdS parasitical absorption, although the CdS layer in both device types was deposited in an identical way. Moreover, ‘rollover’ effects under forward bias contributed significantly to V_{OC} losses. Lastly, both the low R_{SH} and high R_{S} values resulted in low FF values ($< 30\%$). The latter were

ascribed to the higher back contact resistance because of the NW layer roughness or enhanced intrinsic resistance in the CdTe nanowires.

It is probable, however, that the presence of the NWs was parasitical, i.e. light maybe absorbed by the nanowires without any contribution to the photocurrent. NW devices demonstrated a very low average spectral response of $\sim 50\%$, which could not correlate to optical losses. Moreover, devices with various NW length and diameter configurations were evaluated and of all those measured the highest efficiency was achieved for the devices with the shortest nanowires. Thus, the main contribution to the photocurrent could be the absorption of photons in the underlying CdTe buffer layer ($\sim 2\text{ }\mu\text{m}$). This could occur due to fully depleted nanowires, deep levels introduced by impurities and surface recombination and scattering effects. Overall, it was not possible to determine the main contribution to the low PV performance of the NW devices and distinguish between that of the nanowires or the underlying buffer layer. Thus, further investigation using *EBIC* measurements is required in order to evaluate the position of the photovoltaic junction and the nanowire performance. Nevertheless, the NW devices could benefit from deposition techniques that would provide better CdS and ITO conformal growth (e.g. ALD), and the inclusion of a HRT layer. This would act to reduce the electrical effect of shunting paths.

In this chapter, the development of both planar and NW ‘substrate’ CdTe/CdS devices with competitive efficiencies comparable to those of the record devices were shown. The NW superior optical properties and their suitability in PV applications was, also, demonstrated. PV efficiency might be further enhanced both in the planar and NW modified devices by a) replacing CdS with Cd(S,O), b) the inclusion of a HRT layer and c) reducing the forward bias ‘rollover’ effect.

6.8 References

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7 All-sputtered CdTe/CdS solar cells grown on planar and microrod ZnO coated glass substrates

7.1 Introduction

In this chapter, the development and characterisation of CdTe solar cells grown on planar and microrod ZnO coated substrates is reported and the two are compared.

The fabrication techniques for the development of planar and microrod devices, the experiments conducted and the growth conditions are described in Section 7.2. Both the planar and microrod ZnO devices were grown on FTO-coated glass. For the planar devices, ZnO films were deposited by RF magnetron sputtering while the ZnO microrods were deposited electrochemically by collaborators at IK4-CIDETEC, San Sebastian, Spain. The target structure for the microrod devices is shown in Fig. 7.1.

Subsequently, Section 7.3 describes the device optimisation processes and offers an in-depth characterisation of CdTe planar devices. Since planar and microrod devices adopt the same ‘superstrate’ configuration, i.e. glass/TCO/ZnO/CdS/CdTe/Au, this stage was

crucial in the development and optimisation of the microrod devices. Moreover, the high efficiency planar devices were used as a control for the evaluation of the microrod solar cells performance. Initially, the optimisation of the planar solar cell devices is presented in a layer-by-layer study of the ZnO/CdS/CdTe/(back contact) stack with the focus being on the impact of each layers' thickness on the overall device performance. SEM, Raman spectroscopy, *EQE* and *J-V* measurements were used for the individual layers' characterisation and the overall device performance. Next, the application of the novel MgCl₂ activation process and the properties of the post-treatment back surface are discussed. Back surface SEM/EDX elemental analysis and the effect of wet nitric-phosphoric (N-P) acid etching and dry Ar⁺ plasma etching are presented. In the next section, the use of poly(3-hexylthiophene) (P3HT) as a shunt blocking layer and MoO_x/Au, Cu/Au as back contact buffer layers is investigated. Finally, light/ dark and temperature dependent *J-V*, *EQE* and *C-V* measurements of control planar cells having peak efficiencies of up to 13.28% are presented.

Next, the chapter centres on the ZnO microrod-based CdTe solar cells. Firstly, an SEM investigation of the CdTe/CdS microrod devices during the various stages of the fabrication process is presented. Next, the solar cell performance and the factors that influence it are investigated. A peak conversion efficiency of 6.14% was obtained, this

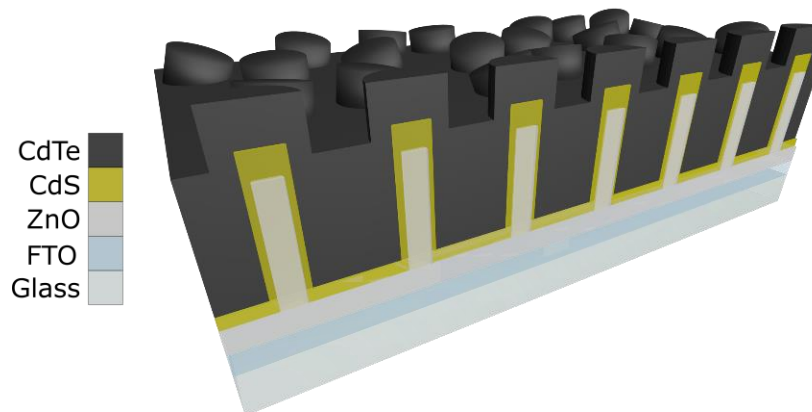


Fig. 7.1 Schematic diagram depicting a cross-section of the CdTe/CdS solar cells based on ZnO microrods

being lower than that of the sputtered planar devices. Cross-sectional FIB-SEM and EBIC studies revealed cavities in the CdTe absorber layer which partly account for the reduced efficiency. The performance shortfall was also investigated by optical transmission and Raman spectroscopy.

7.2 Experimental

In this section, the growth conditions of planar- and microrod-geometry CdTe solar cells are presented together with details of the characterisation techniques used (the reader is referred to Chapter 4 for more background information on the growth and characterisation methods).

7.2.1 Growth conditions of sputtered CdTe solar cells in the planar and microrod geometries

CdTe solar cells were developed on planar and ZnO microrod FTO-coated glass substrates. As mentioned in Section 7, both planar and microrod devices adopt the same glass/TCO/ZnO/CdS/CdTe/Au configuration. Thus, all the individual layers were developed using the same techniques for both device types. The general growth process for the basic planar devices comprised 6 steps, whereas for the microrod devices the first two steps, i.e. substrate preparation and ZnO layer deposition were omitted. Some samples included additional growth steps, such as Cu back contact deposition and in-diffusion, MoO_x intermediate back contact layer evaporation, Ar⁺ or N-P back surface etching or spin-coating of P3HT layers. During all sputtering depositions, initially, the chamber was pumped to a base pressure of 10⁻⁶-10⁻⁷ mbar and non-depositing runs of 5-15 mins in duration were used to clean the sputtering targets. For the devices grown on ZnO nanorods, the thicknesses given are those expected for deposition on an equivalent planar structure and were obtained from the growth times. Local differences

are expected on the microrod structures as compared to the planar substrates and the reader is referred to Section 7.4.1 for cross-sectional SEM views. The following is a description of the sample preparation details organised by device feature. A summary of the sample sets is given in Section 7.2.2.

Substrate preparation: Commercial FTO-coated NSG TEC C15M glass (Pilkington) substrates, 100 mm × 100 mm × 3.2 mm in size, were ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N₂ gun. To remove all surface contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and DI water and dried with a N₂ gun again.

ZnO buffer layer deposition: 80nm thick films were deposited on planar FTO/glass substrates by RF magnetron sputtering. For the process, a ZnO target (3' × 0.25', 99.99% purity, PI-KEM Ltd) was used at room temperature, 150 W power, 5 mTorr Ar pressure for 30 minutes. Profilometry measurements demonstrated a growth rate of 2.7 nm/min.

ZnO microrod deposition: ZnO microrods were developed on 50 mm × 50 mm × 3 mm FTO-coated glass substrates (TEC15, Hartford Glass) by electrochemical deposition. In more detail, the electrolyte solution consisted of ultrapure Millipore water (18 MΩ.cm), 5×10⁻⁴ M ZnCl₂ salt (Fluka, >98% purity) and 2 M KCl (Fluka, >99.5% purity), saturated with bubbled oxygen. In such a process, dissolved O₂ in the electrolytic solution reduces at the cathode to OH⁻ and combines with Zn²⁺ ions to form ZnO¹. The microrod growth mechanism and length was controlled by adjusting the KCl concentration and the charge density applied during the process² to 20 C/cm². All microrod samples were fabricated and provided by Dr. R. Tena-Zaera (IK4-CIDETEC, San Sebastian, Spain).

CdS windows layer deposition: CdS layers were RF sputtered on planar and microrod ZnO coated substrates using CdS targets ($3'' \times 0.25''$, 99.99% purity) from PI-KEM Ltd. 150 W power and 5 mTorr Ar pressure were used and the substrate temperature ranged from 200 to 300°C. Films with varying thickness were obtained by regulating the deposition time from 9 to 72 minutes. AFM and profilometry thickness measurements of planar films demonstrate a growth rate of 3.7 nm/min. For this work, 35 to 265 nm thick films were deposited.

CdTe absorber layer deposition: The deposition of CdTe layers of varied thickness was achieved by RF sputtering material off a $3'' \times 0.25''$, 99.99% pure CdTe target (PI-KEM Ltd). The growth conditions were as follows: 250 – 350°C substrate temperature, 100 W power, 5 – 10 mTorr Ar pressure, 80 – 180 mins duration. The growth rate was measured as 11.3 nm/min using AFM, profilometry and optical techniques.

MgCl₂ treatment: Prior to the MgCl₂ treatment, the samples were cut to 25 mm × 25 mm sizes using in-house made 3D printed jigs and a diamond glass cutter. The MgCl₂ treatment process³ was employed and to the best of our knowledge this is the first report of its application on all-sputtered CdTe solar cells. Commercially available aqueous MgCl₂ solution (Alfa Aesar) was used and three alternative MgCl₂ application methods were investigated: a) spray coating of 0.1-1 M aqueous MgCl₂ solution on the CdTe back surface of the sample, b) spray coating of 1 M aqueous MgCl₂ solution on glass slides, c) 1 M MgCl₂ aqueous solution contained in a glass petri dish. The amount of solution used in each run varied from 25 to 150 µl. For method a) in which the sample had been pre-coated with MgCl₂, the samples were heat-treated in air in the middle of a tube furnace at temperatures from 380 to 440°C for 5 – 60 mins. For methods b) and c), the samples and either the glass slides or petridish sources of MgCl₂ were placed in

close proximity (Fig. 7.2) and heat-treatment was carried out under the same range of conditions. In both methods b) and c) the samples were therefore exposed to MgCl_2 vapour during the-treatment itself. Application method b) yielded the highest efficiencies with a relatively uniform performance across the surface of the samples. In particular, 125 μl of 1 M MgCl_2 aqueous solution was spray coated on the LHS glass slide and 25 μl on the RHS as seen in Fig. 7.2 (left) and annealing temperature was set at 420°C . The optimal annealing time was found to be dependent to the CdTe layer thickness and the geometry of the device (planar or microrod). The samples were rinsed thoroughly with DI water to remove any residues. For the remainder of this chapter this will be considered as the *standard* MgCl_2 processing route.

Back surface etching techniques: Two post- MgCl_2 back surface etching techniques were studied as follows: a) samples were submerged in an N-P etching solution (70% H_3PO_4 , 29% H_2O , 1% HNO_3) for 2 to 15 secs followed by a DI water rinse, b) samples were Ar^+ plasma etched in the AJA sputtering equipment at room temperature using 10 mTorr of Ar pressure and a DC power of 25 W for times between 30 secs and 5 mins

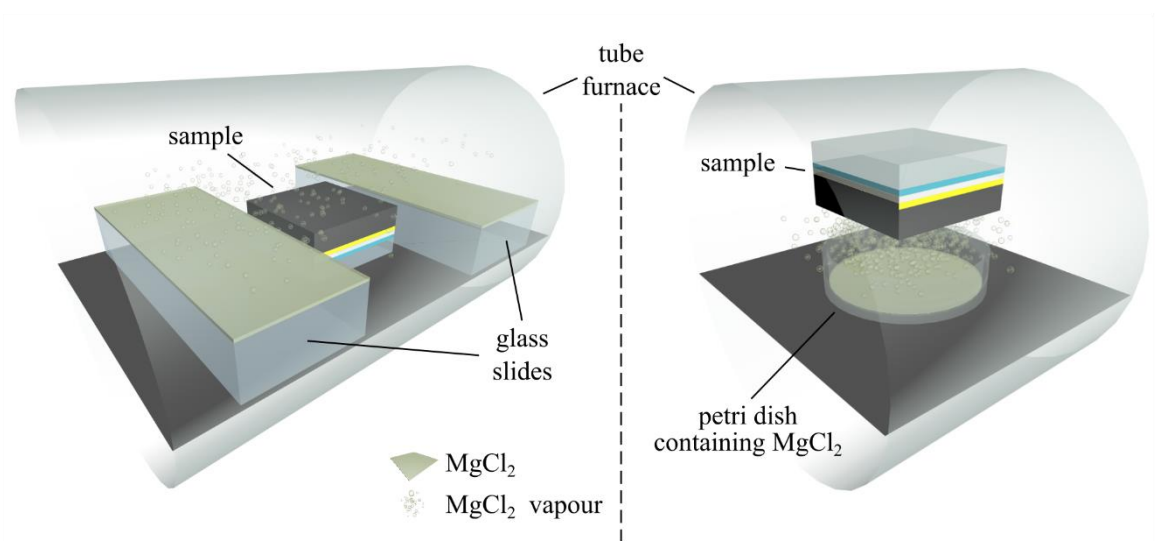


Fig. 7.2 Sample geometries for methods b (left) and c (right) in the text used for exposing solar cell samples to MgCl_2 vapour in a tube furnace during heat-treatment

(etching rate 7 nm/min). Apart from cleansing the back surface from residues and oxides, this wet or dry etching was employed to create a Te- rich layer, which is reported to demonstrate enhanced p-type conductivity and a beneficial effect on the solar cell performance⁴⁻⁶.

Au, Cu/Au and MoO_x/Au back-contact layers deposition: Devices with different back contact layer stacks, i.e. Au, Cu/Au and MoO_x/Au were fabricated. Although Cu is commonly used to rectify CdTe back contact issues and improve the device performance, it is also found to induce cell degradation over time⁷. MoO_x is an alternative material that is reported to reduce the forward bias ‘rollover’ when used as a back contact buffer layer^{8,9}. Au, Cu and MoO_x layers were thermally evaporated at room temperature at a base pressure of 10⁻⁵ mbar. All contacts were deposited in a matrix fashion by using in-house 3D printed masks with rectangular apertures. The contact size was determined by analysing high-resolution photographs using the ImageJ¹⁰ software. Initially a pixel/mm scale was set using a high-precision ruler and the area of 50 contacts was measured. The average contact size for the samples with Cu/Au or MoO_x/Au back contacts was 0.12 cm² and for the samples with Au back contacts 0.134 cm². The thickness of the Au layers was 40 nm, the Cu layers from 3 to 7 nm and the MoO_x layers ranged from 5 to 20 nm. The corresponding evaporation rates for Au, Cu and MoO_x were maintained at 8 Å/s, 0.2 Å/s and 0.2 Å/s. Thickness measurements were carried out using AFM, profilometry and ellipsometry techniques. In order to promote the Cu in-diffusion, the samples with the Cu/Au back contacts were annealed in air at 150°C for 15-45 mins. The MoO_x depositions were performed by Mr. T. Baines, University of Liverpool.

P3HT layer deposition: The hypothesis that P3HT layers can be used as shunt blocking layers was investigated. In general, P3HT is commonly used in perovskite solar cells as a hole transport layer with high hole mobilities¹¹. 15 wt.% P3HT in chlorobenzene solutions were prepared inside a glovebox under a controlled N₂ pressure. The solutions were annealed at 75°C for 15 minutes and filtered. 25-300 µl of P3HT solutions were spin-coated on planar and microrod samples using a 2-step spin-coating process: step a) rotation 1000 rpm, acceleration 1000 rpm/s, 10 secs, step b) rotation 4000 rpm, acceleration 1200 rpm/s, 30 secs. The solution was dynamically cast onto the sample's surface during the first seconds of step a. The samples were annealed at 150°C for 15 minutes to allow the solvent to completely evaporate.

7.2.2 Sample sets

Overall, ~ 300 planar device samples with 9-16 contacts/sample and 32 microrod device samples with 16 contacts/sample, 25 mm × 25 mm in size, were fabricated for the experiments of this chapter. All devices adopted the 'superstrate' configuration, i.e. TEC/ZnO/CdS/CdTe/(back contact). The sputtering conditions used for the fabrication of the sample sets of sections 7.3 and 7.4 are summarised in Table 7.1. All samples had been subjected to the standard MgCl₂ process as described in 7.2.1. All planar devices included an 80-nm thick ZnO layer. Specific details for the sample sets reported in sections 7.3 and 7.4 are given below.

Table 7.1 Optimal sputtering conditions for the ZnO, CdS and CdTe layers used in samples of sections 7.3 and 7.4

Layer	Temperature (°C)	Pressure (mTorr)	Power (W)
ZnO	RT	5	150
CdS	200	5	60
CdTe	300	10	100

The effect of the CdS window layer (Section 7.3.1): All devices included a 1.8 μm thick CdTe layer and the CdS layer thickness varied between 35 and 90 nm (Table 7.3, Section 7.3.1). 5 nm of Cu and 40 nm of Au were thermally evaporated using the 0.12 cm^2 contact masks. The devices were completed with a final annealing step at 150°C for 25 mins in air.

The effect of the CdTe absorber layer (Section 7.3.2): All devices incorporated a 90 nm thick CdS window layer, while the CdTe absorber layer thickness ranged from 0.9 to 1.6 μm (Table 7.4, Section 7.3.2). The samples were processed using the standard MgCl_2 step for 11 ('CdTe09'), 13 ('CdTe13') and 14 mins ('CdTe16'). 5 nm of Cu and 40 nm of Au were thermally evaporated using the 0.12 cm^2 contact mask aperture areas. The devices were annealed at 150°C for 25 mins in air.

Post- MgCl_2 back surface characterisation and etching studies (Section 7.3.3): The samples used for the back-surface analysis (Table 7.5, Section 7.3.3.1) and the investigation of the two alternative etching techniques (Table 7.6, Section 7.3.3.2 and Table 7.7, Section 7.3.3.3) had 45 nm thick CdS layers and 1.8 μm thick CdTe layers. The standard MgCl_2 treatment was performed for 15 mins. The etching intervals varied from 2 to 12 secs for the N-P etching and from 1 to 5 mins for the plasma etching. Au contacts were thermally evaporated with a final thickness of 40 nm and an area of 0.134 cm^2 .

Study of the Cu/Au back contact behaviour of planar CdTe/CdS solar cells (Section 7.3.4.1): The devices used in this section were fabricated with 45 nm thick CdS window layers, 1.8 μm thick CdTe absorber layers and Cu/Au back contacts. Cu layer with varying thickness (Table 7.9, Section 7.3.4.1) and 40 nm thick Au layers were thermally

evaporated using the 0.12 cm² contact mask aperture areas. After the development of the back contacts, the samples were annealed in air at 150°C for 25 mins.

Study of the MoO_x/Au back contact behaviour of planar CdTe/CdS solar cells (Section 7.3.4.2): Thermally evaporated MoO_x layers were investigated as an alternative back contact buffer layer to Cu. For this purpose, three devices with 45 nm thick CdS window layers, 1.8 µm thick CdTe absorber layers, Au (control sample) and MoO_x/Au back contacts were fabricated. The MoO_x layers were 5 nm ('MoO_x5') and 10 nm ('MoO_x10') thick (Table 7.10, Section 7.3.4.2). All contacts were developed using the 0.12 cm² contact mask aperture areas.

Test of P3HT as a shunt-blocking layer on planar CdTe/CdS solar cells (Section 7.3.4.3): Planar devices with 90 nm thick CdS and 1 µm thick CdTe layers were fabricated. For the evaluation of the impact of the P3HT layer, the deposited CdTe layers were considerably thinner when compared to other experiments of this chapter. Thin CdTe layers exhibit lower degree of coverage and a higher density of shunting paths/voids. Prior to the Au back contact deposition, P3HT layers were spin-coated on the CdTe back surface. In particular, 25µl of P3HT were spin-coated on sample 'P3HT25', 50µl on sample 'P3HT50' and 75µl on sample 'P3HT75', while sample 'P3HT0' had no P3HT incorporated (Table 7.11, Section 7.3.4.3). 40 nm thick Au back contact layers were thermally evaporated using the 0.12 cm² contact mask aperture areas.

Electrical characterisation of highest efficiency planar devices (sections 7.3.5 and 7.4.2): Detailed characterisation was conducted on examples of the best-performing planar and microrod devices. The layer thicknesses for these devices are reported in Table 7.2.

Table 7.2 Growth conditions for the highest performing planar and microrod CdTe/CdS devices

	Planar devices	Microrod devices
ZnO (nm)	80	-
CdS (nm)	45	90
CdTe (nm)	1800	2000
Cu (nm)	5	5
Au (nm)	40	40
Contact area (cm ²)	0.12	0.12
Final anneal	25 mins @ 150°C	35 mins @ 150°C

SEM/EDX investigation of the CdTe/CdS microrod devices development (Section 7.4.1): SEM plain, angled and cross-sectional views of microrod CdTe/CdS devices during the various deposition steps were acquired. Moreover, an SEM/EDX analysis of the back surface of MgCl₂ treated microrod devices was performed. More details for the samples used in this part are given on Table 7.13 (Section 7.4.1).

Comparison of planar and microrod CdTe/CdS devices by means of Raman and optical spectroscopy (Section 7.4.3): Raman and optical spectroscopy measurements of planar and microrod CdTe/CdS devices were performed and compared. As-grown ZnO microrods and ZnO films, CdS coated and complete microrod and planar devices were used for the purposes of this work. Details of the individual layers' thickness are given on Table 7.16 and Table 7.15 of Section 7.4.3.

7.2.3 Characterisation techniques

The samples in this chapter were characterised using techniques that are described more fully in Chapter 4. Briefly the methods used were: light, dark and temperature dependent *J-V* measurement, *EQE*, *C-V*, SEM/EDX and SEM/EBIC of planar and FIB cross sections, optical transmittance/reflectance and Raman spectroscopy. All measurements

were made by the author except the EBIC which was performed by Mr L Bowen at the GJ Russell Electron Microscope Facility at Durham University on a Hitachi SU70 SEM with a Matelect ISM5 specimen current amplifier.

7.3 Planar CdTe/CdS solar cell devices

7.3.1 The effect of the CdS window layer thickness

In this section, results on the impact of the CdS layer thickness on the PV performance of planar CdTe devices are presented. Typical J - V curves of the best performing contacts of devices with 35, 45 and 90 nm thick CdS layers are demonstrated in Fig. 7.3a. The peak conversion efficiencies are shown on Table 7.3.

To determine the optimum CdS layer thickness, a statistical analysis of the individual PV parameters, η , V_{OC} , J_{SC} and FF , for all the samples contacts was performed. The results are shown in the box plots of Fig. 7.4. Although all four plots demonstrate a

Table 7.3 Peak and averages efficiencies of samples with CdS layers of varied thicknesses

Sample	CdS thickness (nm)	Peak efficiency (%)	Avg. efficiency (%)
CdS35	35	8.85	7.44
CdS45	45	13.21	10.95
CdS90	90	11.71	8.55

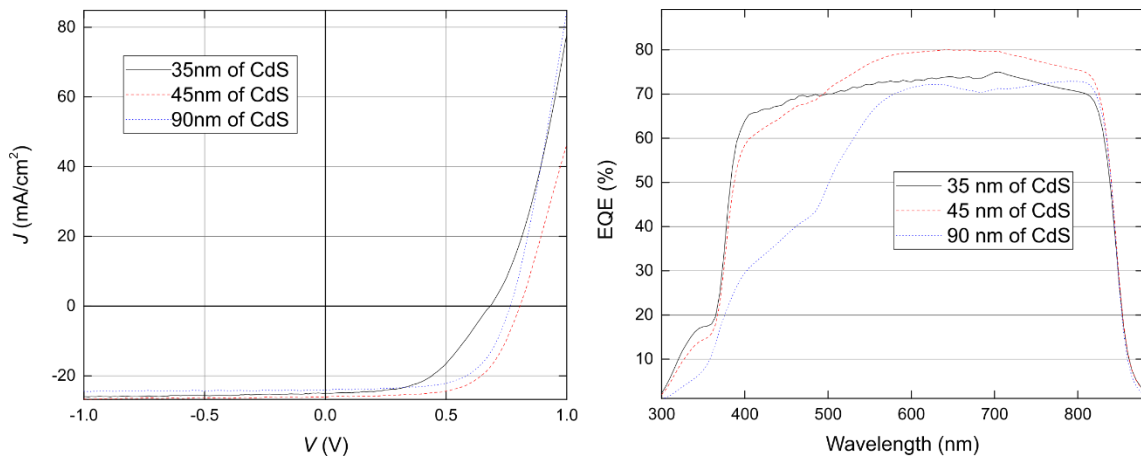


Fig. 7.3 J - V (a) and EQE (b) curves of best CdTe/CdS planar devices contacts with varying CdS layer thickness

noticeable spread, the ‘CdS45’ device outperforms the other two in every measured quantity. Evaluation of the statistical analysis lead to two main observable trends: a) thinning of the CdS layer below 45 nm results in decrease of both V_{OC} and FF , while b) thicker CdS layers have a detrimental impact on the J_{SC} .

EQE measurements of the same devices are shown in Fig. 7.3 (right). In accordance with the J - V results, thinning of the CdS layer leads to a gradual increase of the EQE response for wavelengths less than ~ 500 nm (i.e. above the CdS absorption edge). However, EQE losses are observed for wavelengths above 500 nm when the CdS layer becomes thinner than 45 nm.

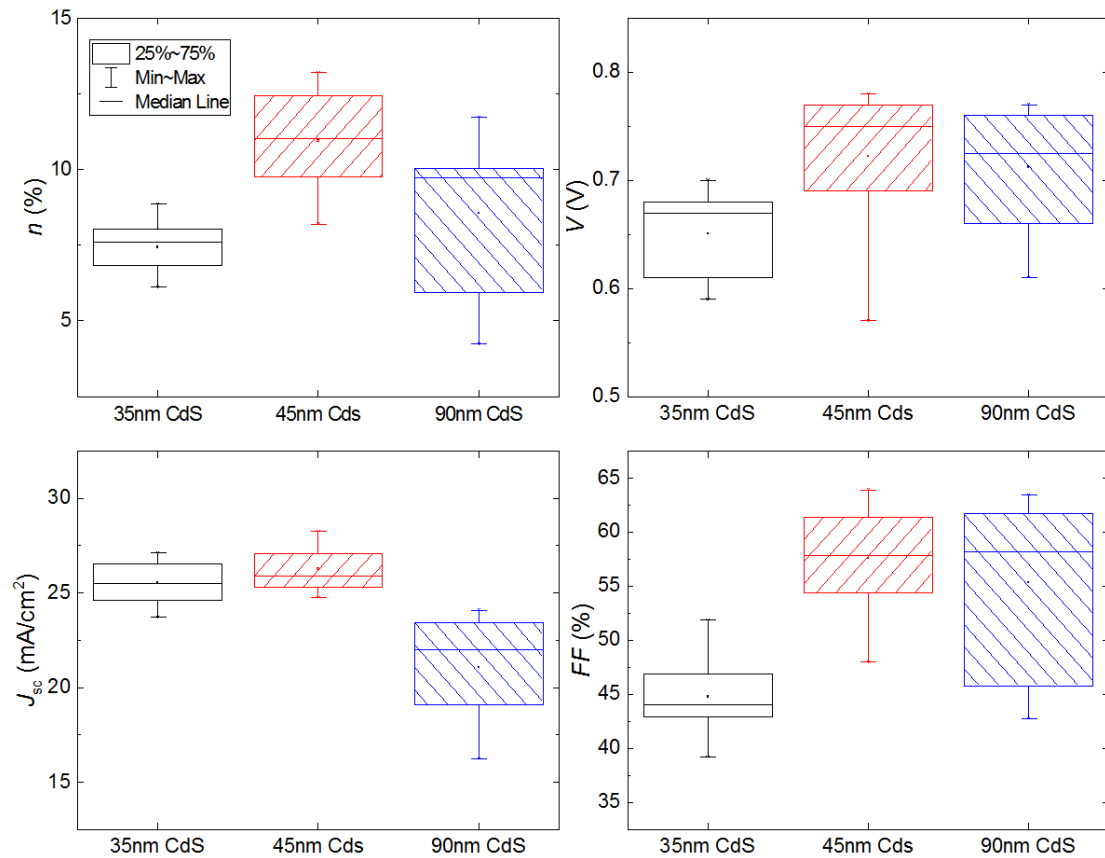


Fig. 7.4 Statistical analysis of the PV parameters η , V_{OC} , J_{SC} , FF for planar devices with 35, 45 and 90 nm thick CdS layer. The boxplots sample size is $N = 14$

7.3.2 The effect of the CdTe absorber layer thickness

PV performance results of planar CdTe devices with varying CdTe thicknesses are presented in this section. J - V and EQE curves of the best performing contacts are shown in Fig. 7.5 and a statistical analysis of the PV performance parameters η , V_{OC} , J_{SC} , FF as a function of varying CdTe thickness is shown in Fig. 7.6.

Peak conversion efficiencies of the highest efficiency contacts were measured equal to 8.31% for sample ‘CdTe09’, 9.99% for sample ‘CdTe13’ and 11.71% for sample ‘CdTe16’ (Fig. 7.5a). Evaluation of the J - V and EQE measurements from the highest efficiency contacts for each device run show an increase in all device parameters with increasing CdTe thickness. R_S and R_{SH} values (Table 7.4) show that increase of CdTe thickness above $1.6\mu\text{m}$ results in a significant increase of R_{SH} . Conversely, R_S values decrease only marginally.

Table 7.4 Peak and average efficiencies, R_S and R_{SH} values of the CdTe/CdS planar device samples with varying CdTe layer thickness

Sample	CdTe (nm)	η_{max} (%)	η_{avg} (%)	R_{SH} ($\Omega.\text{cm}^2$)	R_S ($\Omega.\text{cm}^2$)
CdTe09	900	8.31	6.2	694 ± 62	6.5 ± 0.3
CdTe13	1300	9.99	9.23	737 ± 46	6.5 ± 0.4
CdTe16	1600	11.71	10.23	2815 ± 898	4.8 ± 0.3

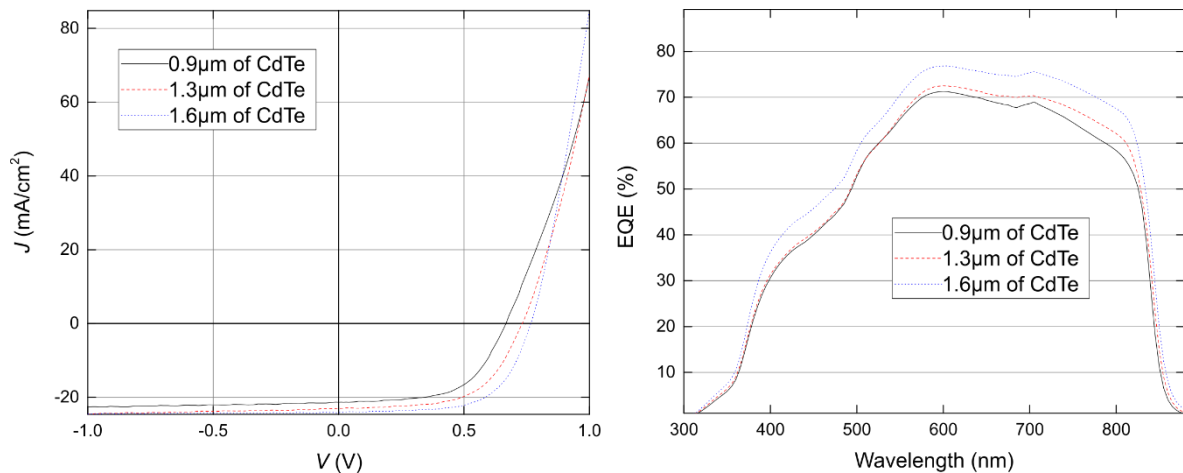


Fig. 7.5 J - V (a) and EQE (b) curves of the highest efficiency CdTe/CdS planar devices contacts with varying CdTe layer thickness

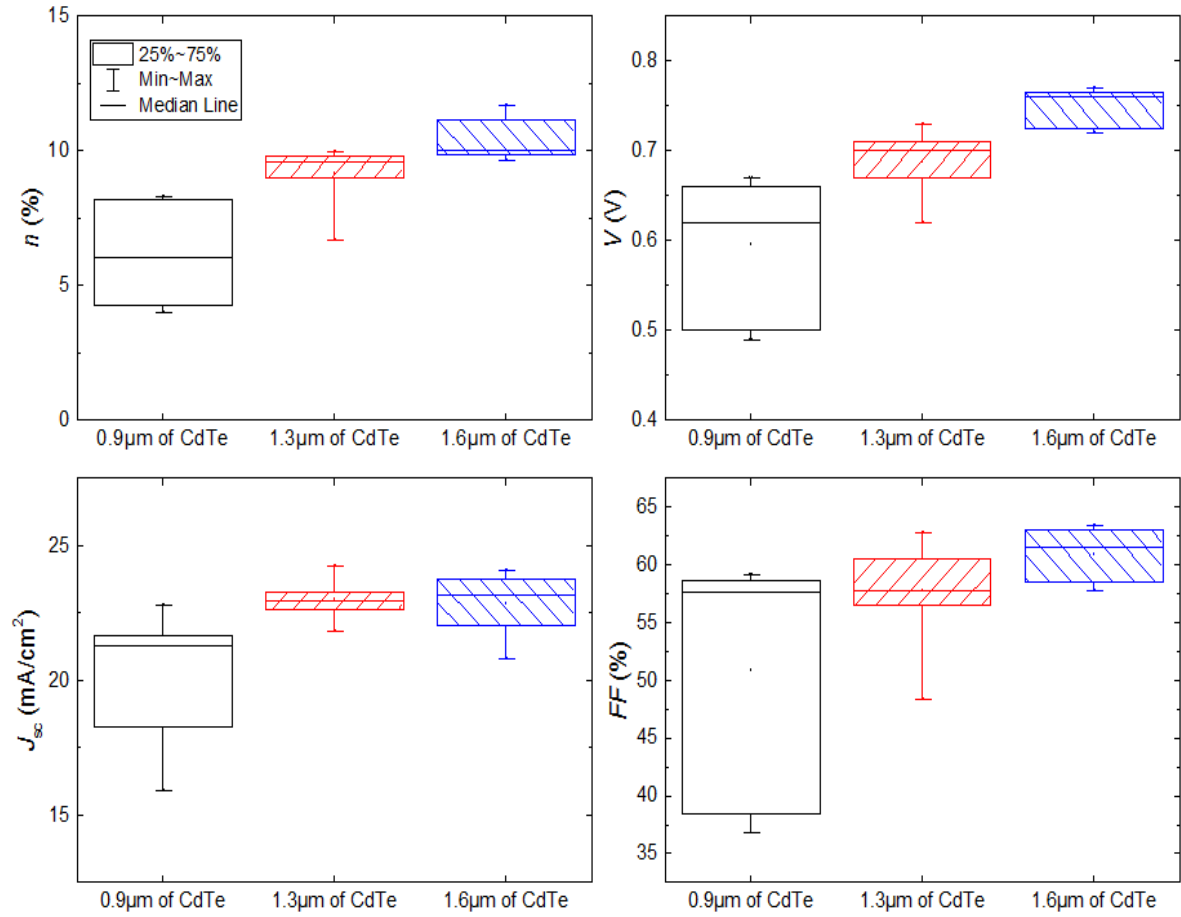


Fig. 7.6 Statistical analysis of the PV parameters η , V_{oc} , J_{sc} , FF for devices with 0.9, 1.3 and 1.6 μm thick CdTe layers. The boxplot sample size is $N = 10$

Further assessment of the performance parameters (Fig. 7.6) reveals similar trends overall despite the data spread: η , V_{oc} and FF increase with increasing CdTe thickness. In contrast, the short-circuit current densities reveal a different behaviour; initially J_{sc} increases to a peak for sample ‘CdTe13’ and then decreases with increasing CdTe thickness. The higher R_s values of thicker CdTe layers may limit J_{sc} (although this was not observed for the best performing contacts of Fig. 7.5). Overall, the open-circuit voltage appears to be the dominant PV parameter and it affects the devices power conversion efficiency strongly with increasing CdTe thickness.

7.3.3 *Post-MgCl₂ back surface characterisation and etching studies*

This section presents an SEM/EDX study of the effects of MgCl₂ treatment and subsequent etching using wet chemical and dry plasma etching techniques.

7.3.3.1 *Post-MgCl₂ back surface analysis*

In Fig. 7.7, SEM micrographs of the CdTe surface morphology are shown depicting the recrystallization effect of the MgCl₂ treatment. Image analysis of the untreated samples' micrographs with the ImageJ¹⁰ software demonstrate grain sizes that range from tens to some hundreds of nanometres. Moreover, large gaps in the grain structure are evident. As-grown devices with no MgCl₂ activation treatment performed, had very poor conversion efficiencies (< 1%). Fig. 7.7 (right) illustrates the back surface of CdTe after the MgCl₂ treatment. In this case, crystallites with sizes in the micron regime and the formation of a more compact film is observed.

Representative Raman spectra of as-deposited and MgCl₂ treated samples are shown In Fig. 7.8. All samples demonstrated good homogeneity without significant changes in the spectra obtained from various points. A wide number of distinctive features can be observed. These are located at 61 ± 2 , 73 ± 2 , 97 ± 2 , 125 ± 2 , 146 ± 3 and 168 ± 2 cm⁻¹

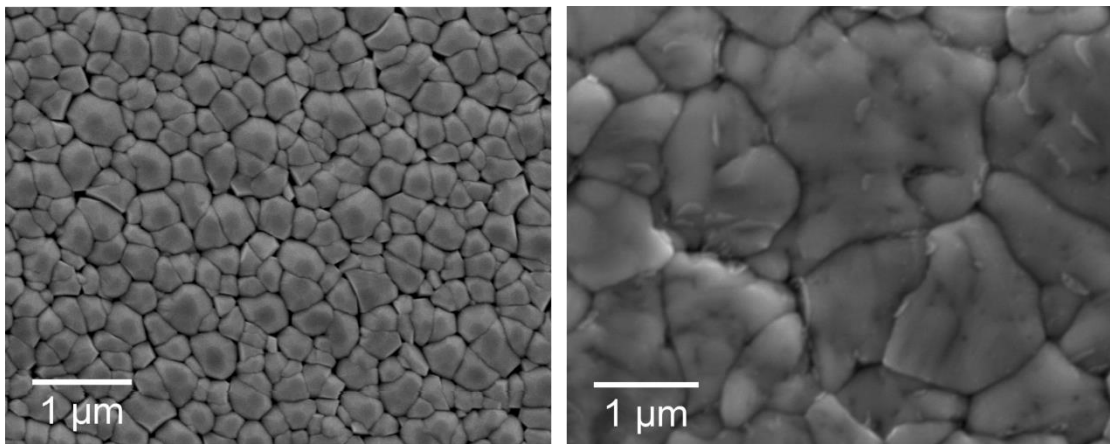


Fig. 7.7 SEM micrograph of the CdTe back surface before (left) and after (right) the MgCl₂ activation process

¹ (average values). Such features can be assigned to active optical and vibrational modes of Te, TeO₂ and CdTe. In particular, the weak shoulder at 168 cm⁻¹ can be ascribed to CdTe LO phonon mode, the peak at 146 cm⁻¹ to a superposition of CdTe TO phonon mode and *E* symmetry vibrational mode of Te and the peak at 125 cm⁻¹ to the A₁ symmetry vibrational mode of Te^{12,13}. As can be seen, the 168 cm⁻¹ shoulder is relatively broad extending to higher frequencies. The breadth of this LO CdTe phonon mode is reported to relate to acoustic phonons, surface-induced vibrational modes, disorder-activated phonon modes or elemental Te nanocrystallites¹³. Low frequency features of the spectra below 100 cm⁻¹ can be ascribed to TeO₂¹⁴ and Te^{15–17} vibrational modes and CdTe LO-TA mode¹².

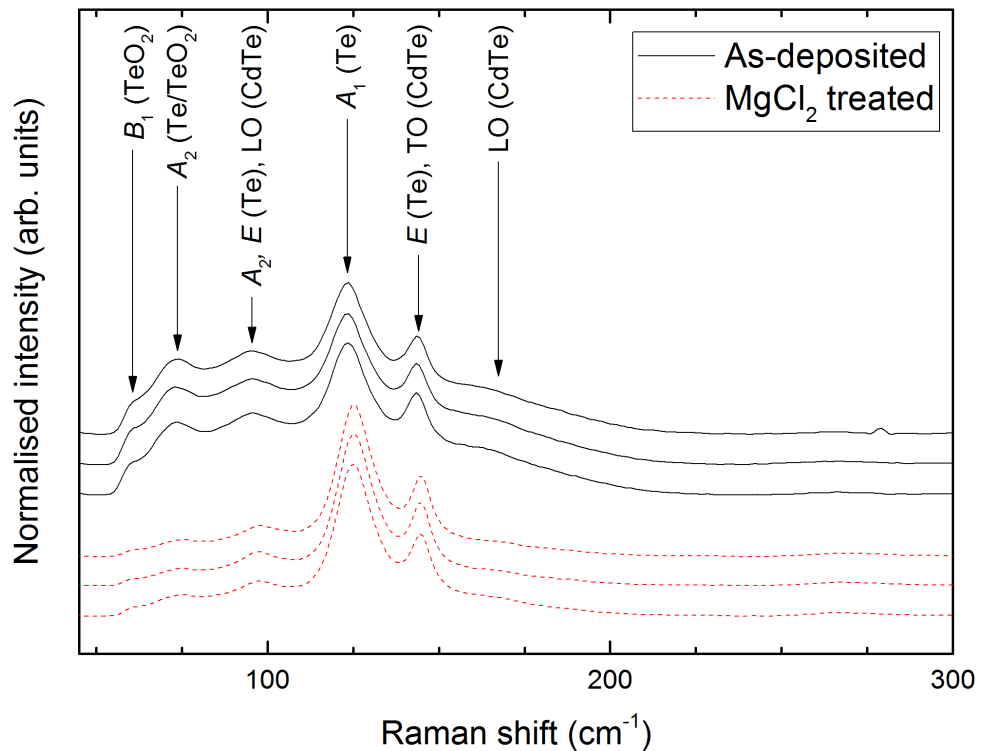


Fig. 7.8 Representative normalised Raman spectra of as-deposited and MgCl₂ treated samples. Various points on the samples' surface were used for the data acquisition, showing insignificant changes and a good sample homogeneity. The candidate optical and vibrational modes are assigned above the characteristic peaks and shoulders

Table 7.5 Back surface EDX analysis of the CdTe surfaces of MgCl_2 treated planar devices. The areas used for the EDX data acquisition are shown in Fig. 7.9.

Sample	O (at.%)	Mg (at.%)	Cl (at.%)	Cd (at.%)	Te (at.%)
Sample A	0	0.05	0.41	50.91	48.64
Sample B	0	0.15	0.24	49.61	50
Sample C	10.2	0	1.86	45.35	42.6

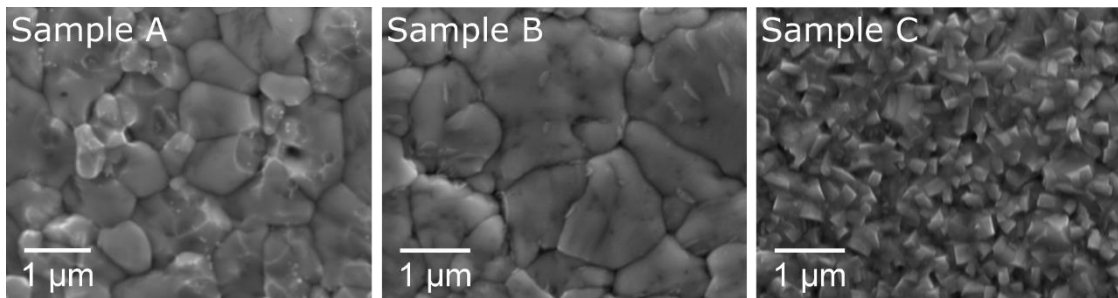


Fig. 7.9 SEM micrographs of the CdTe surfaces of samples A, B and C showing areas with different morphologies. All samples were fabricated and MgCl_2 treated in the same way

SEM investigation of the CdTe back surface morphology of MgCl_2 treated samples revealed areas with residues/contamination from the activation process. The elemental composition of such areas was studied using SEM/EDX analysis on three MgCl_2 treated samples. EDX results are presented in Table 7.5 and the areas used for the data acquisition are shown in Fig. 7.9. A small amount of Mg residues was detected on samples A and B, while Cl can be traced in all three samples. On the contrary, Sample C demonstrates a much more evident source of surface contamination with a higher Cl concentration and an oxygen content of ~ 10 at.%. Such impurities may account for performance deviations across the sample's contacts and act as a limiting factor for the power conversion efficiency of the solar cell devices.

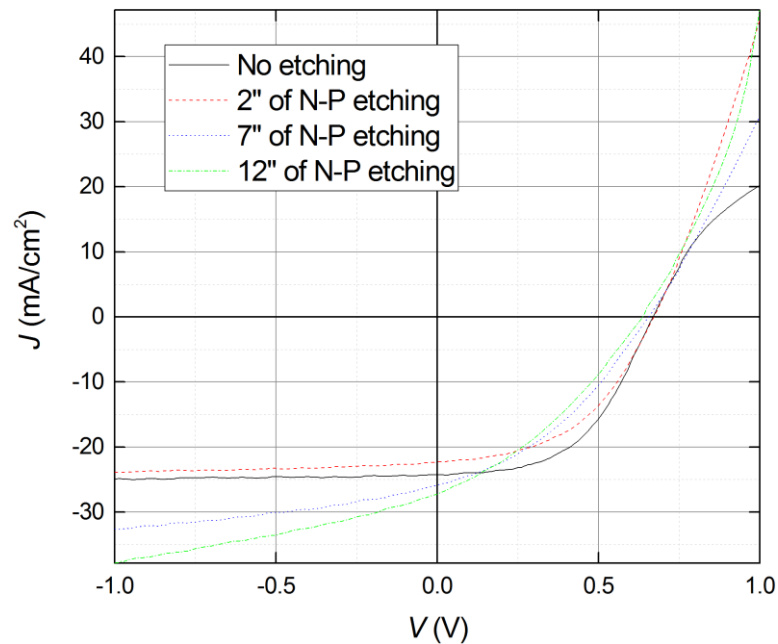
7.3.3.2 The effect of N-P wet etching

In this section, results on the impact of a wet nitric-phosphoric etching process on the back surface and the overall PV performance of planar CdTe/CdS devices are presented.

Table 7.6 Sample set used for the evaluation of the N-P etching impact on the PV performance of planar CdTe/CdS devices

Sample	N-P etching time (secs)	Peak efficiency (%)	Avg. efficiency (%)
NP0	0	8.32	7.18
NP2	2	7.18	4.74
NP7	7	6.75	4.87
NP12	12	5.48	3.43

An as-grown control sample and three samples subjected to different etching times were used (Table 7.6). J - V measurements of the best performing contacts (Fig. 7.10) and statistical analysis of all four PV parameters for all the samples' contacts (Fig. 7.11) show a performance decrease with increasing etching time intervals. The dominant performance limiting factor appears to be the FF , which is caused by a significant decrease in the R_{SH} values of the etched samples. SEM investigation of the surface morphology of the etched samples reveal the development of, cracks and protuberances, which increase in size with increasing etching time (Fig. 7.12). These features constitute severe film defects and result in extensive number of shunting pathways, which account for the poor FF and R_{SH} values.

Fig. 7.10 Best contact J - V curves of samples 'NP0', 'NP2', 'NP7' and 'NP12'

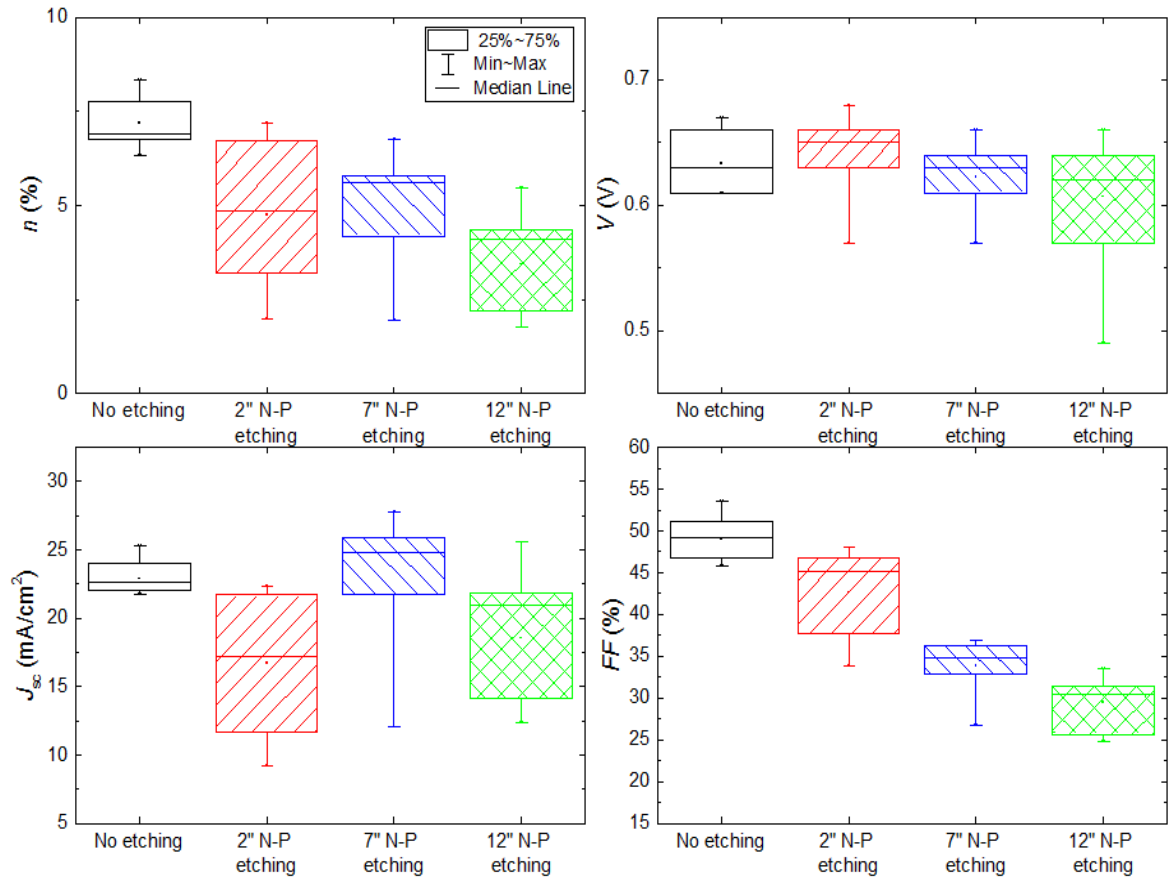


Fig. 7.11 Statistical analysis of the PV parameters η , V_{oc} , J_{sc} , FF for devices with varying N-P etching times. $N = 14$ for each processing time

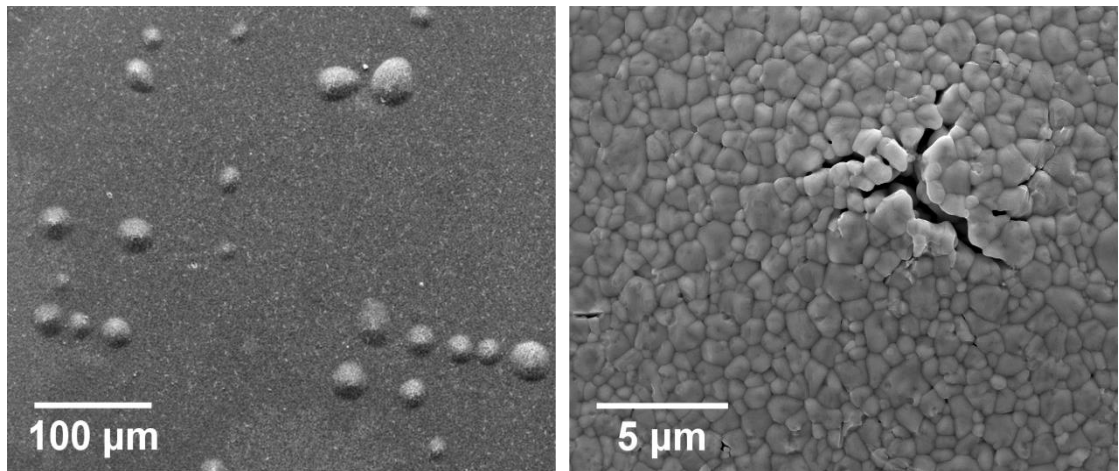


Fig. 7.12 SEM images of the CdTe surface of N-P etched sample 'NP12'. Left: low magnification micrograph illustrating protuberances on the surface of the sample. Right: high magnification image of a protuberance revealing the presence of defects in the CdTe

7.3.3.3 The effect of Ar^+ plasma dry etching

Ar^+ plasma dry etching was investigated as an alternative to the N-P wet etching of Section 7.3.3.2. There was one control sample and three etched samples for (1, 3 and 5 minutes). All three etched devices demonstrated power conversion efficiencies below 2%, as can be seen in Fig. 7.13 and Fig. 7.14. The J - V curves of the etched samples demonstrate pronounced ‘rollover’ effects under forward bias (samples ‘Ar1’, ‘Ar3’) and S-kinks (sample ‘Ar5’). Such distortions can be ascribed to carrier extraction barriers or high R_S values due defects or impurities on the back surface of the device.

Table 7.7 Peak and average efficiencies of Ar^+ plasma etched samples for different etching times

Sample	Plasma etching (mins)	Peak efficiency (%)	Avg. efficiency (%)
Ar0	0	7.18	8.32
Ar1	1	1.01	1.72
Ar3	3	1.07	1.59
Ar5	5	0.99	1.34

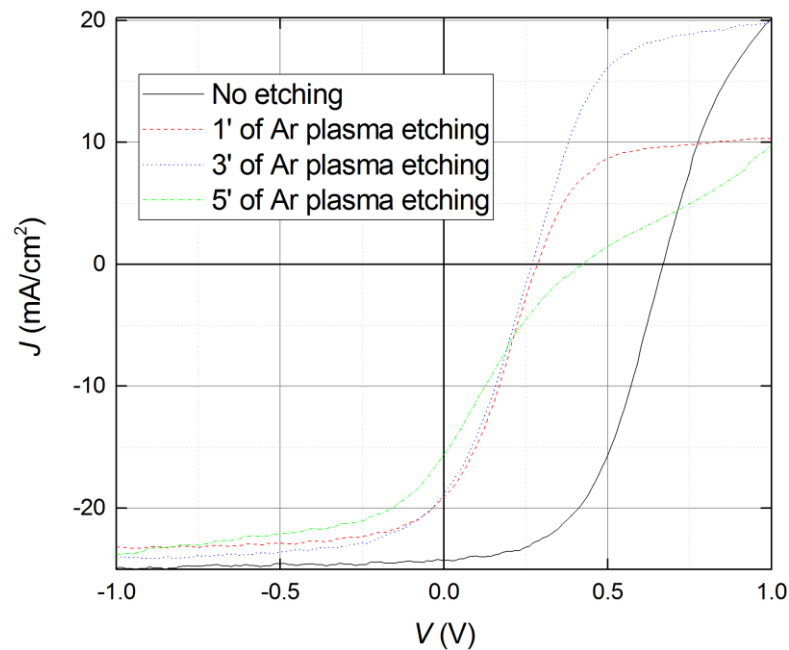


Fig. 7.13 Best contacts J - V curves of dry etched planar CdTe samples ‘Ar0’, ‘Ar1’, ‘Ar3’ and ‘Ar5’

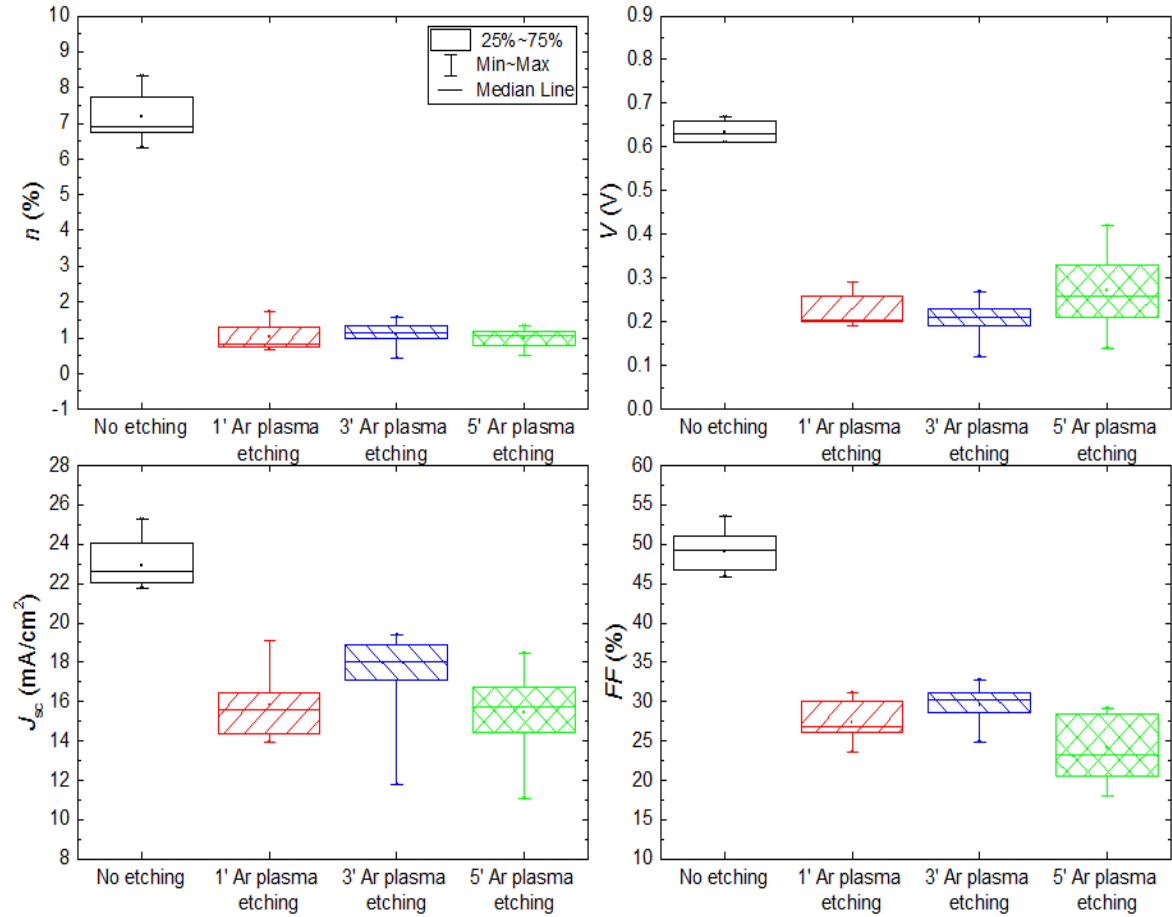


Fig. 7.14 Statistical analysis of the PV parameters η , V_{OC} , J_{SC} , FF for devices with varying Ar^+ plasma etching intervals. $N = 11$ for each processing time

SEM images of the samples etched for 3 and 5 minutes are shown in Fig. 7.15. While sample ‘Ar1’ did not depict any noticeable surface features (not shown here), surface irregularities were detected on samples ‘Ar3’ and ‘Ar5’. In order to trace the origin of these features SEM/EDX analysis was performed and the results are shown on Table 7.8. The EDX spectra of the small (< 200 nm) spheres in sample ‘Ar3’ revealed no impurities. However, the approximate Grün electron range ($\rho_{CdTe} = 5.85$ gr/cm³, $V_{ac.} = 15$ kV), the penetration depth of the primary electrons, is close to a micron. Therefore, it is highly probable that the signal coming from such small surface features is not detectable. On the contrary, a mixture of differently sized elongated structures was observed on the surface of sample ‘Ar5’. Similarly to ‘Ar3’, EDX spectra of the small

Table 7.8 Back surface EDX analysis of plasma etched samples ‘Ar3’ and ‘Ar5’. Fig. 7.15 shows the areas used for the EDX data acquisition

Spectrum	Etching time (mins)	O (at.%)	Cl (at.%)	Cd (at.%)	Te (at.%)
Sp. 3-1	3	0	0	52.48	47.52
Sp. 3-2		0	0	51.83	48.17
Sp. 3-3		0	0	50.36	49.64
Sp. 5-1	5	20.19	4.55	38.76	36.5
Sp. 5-2		0	0	49.15	50.85
Sp. 5-3		0	0	49.31	50.69
Sp. 5-4		38.85	11.08	28.23	21.84

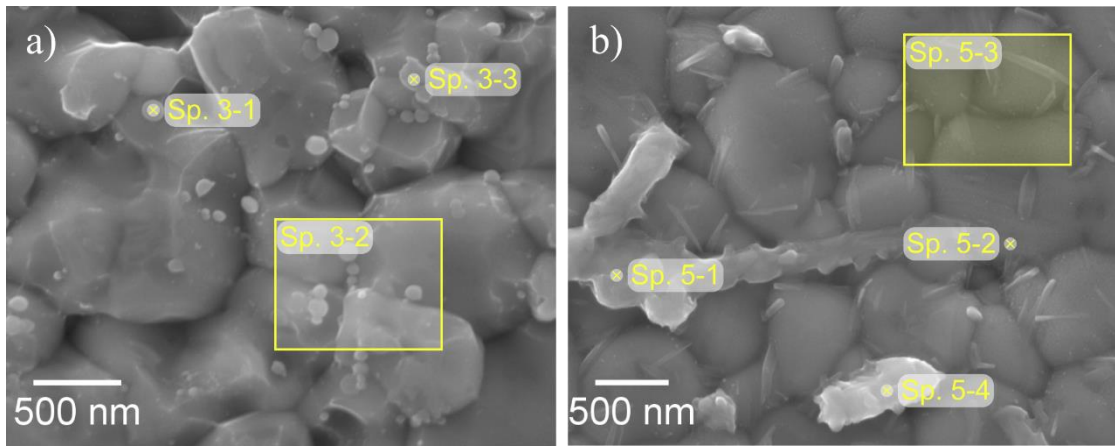


Fig. 7.15 SEM micrographs of the CdTe surfaces of the plasma etched samples ‘Ar3’ (a) and ‘Ar5’ (b). The sites where point and area EDX analysis was performed are marked

features contained only peaks from Cd and Te. However, spectra ‘Sp. 5-1’ and ‘Sp. 5-4’ demonstrated concentrations of oxygen and chlorine, which are much higher when compared to unetched samples (Table 7.5). Clearly, Ar^+ plasma etching results in a defective back material with a high concentration of surface impurities. that has a severe effect on the PV performance of the planar CdTe/CdS devices.

7.3.4 Back contact buffer layers

Results of the effects of Cu/Au, MoO_x/Au and P3HT/Au back contacts are presented in this section.

7.3.4.1 Study of the Cu/Au back contact behaviour of planar CdTe/CdS solar cells

The PV performance of devices incorporating 3, 5 and 7 nm thick Cu layers (Table 7.9) was investigated and compared to that of a nominally Cu-free device. J - V curves of the best contacts are presented in Fig. 7.16 and the extracted η , V_{OC} , J_{SC} , FF values are presented in Fig. 7.17. Cu-free devices demonstrated relatively low J_{SC} values and

Table 7.9 Peak and averages efficiencies of samples with Cu layers of varied thicknesses. The devices have a Cu/Au back contact layer stack

Sample	Cu (nm)	Peak efficiency (%)	Avg. efficiency (%)
Cu0	0	10.46	9.75
Cu3	3	11.26	9.12
Cu5	5	12.01	10.21
Cu7	7	11.43	9.46

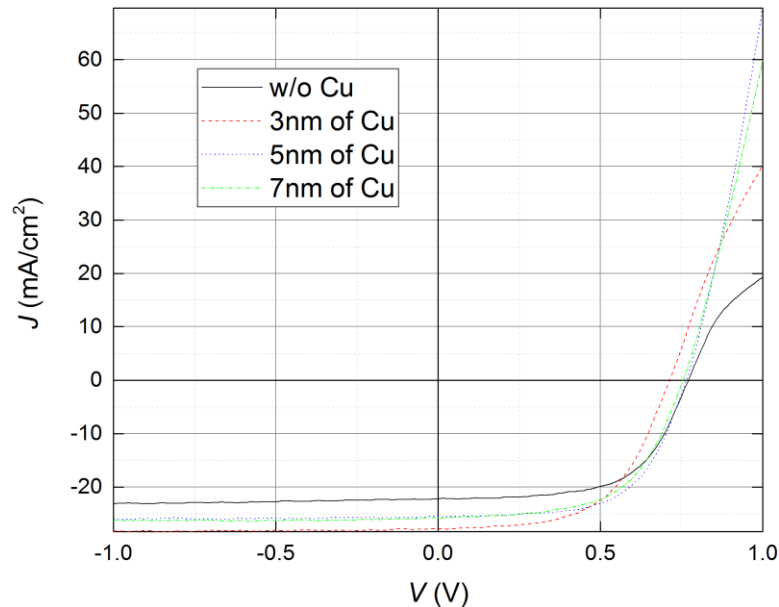


Fig. 7.16 J - V curves of Cu-free planar CdTe/CdS devices and devices incorporating 3, 5 and 7 nm thick Cu layers

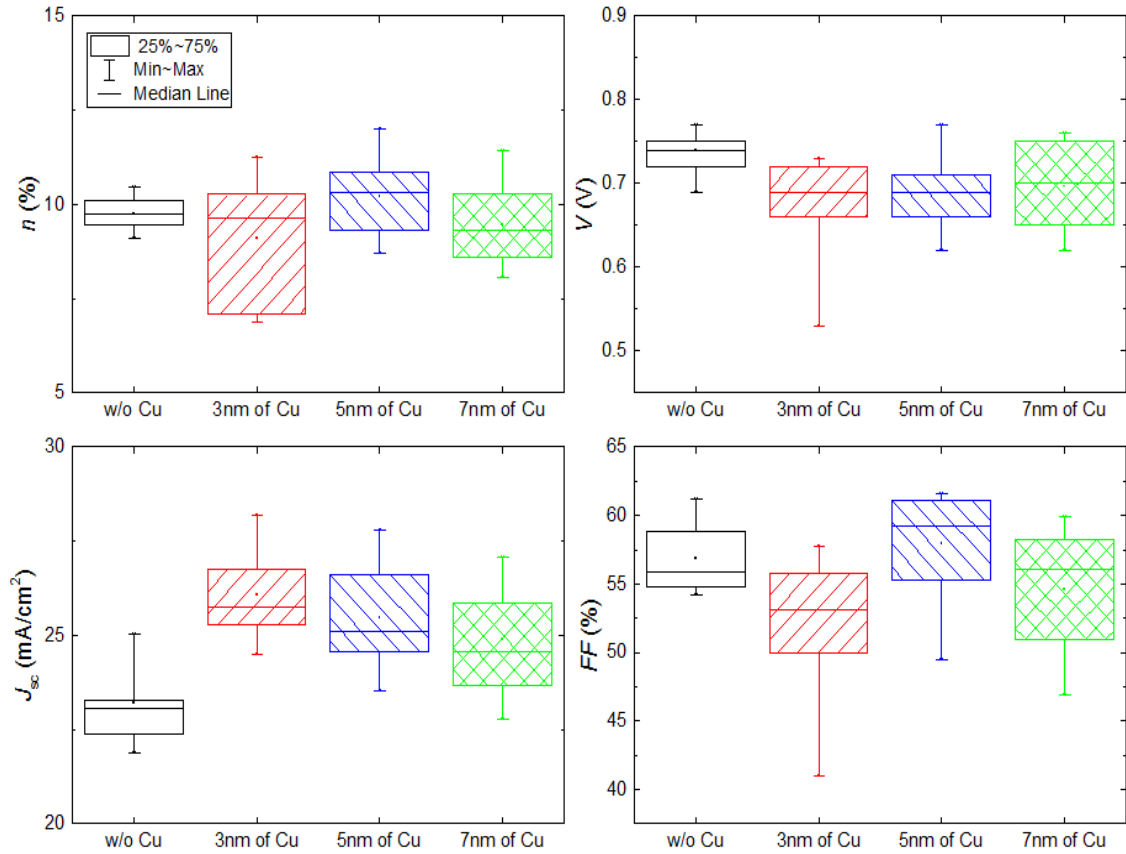


Fig. 7.17 Statistical analysis of the PV parameters η , V_{OC} , J_{SC} , FF for devices with varying Cu back contact layer thickness. Sample size for each boxplot is $N = 13$

suffered from the back contact ‘rollover’ effect of the J - V curve under high forward bias. Addition of Cu led to gradual diminishing of the back contact ‘rollover’ effect, decrease in the series resistance of the devices and increased values of J_{SC} . Although incorporation of thin Cu layers seems to be beneficial to the PV performance, thicker Cu layers as in sample ‘Cu7’ resulted in decreased device performance. The optimal Cu layer thickness was 5 nm.

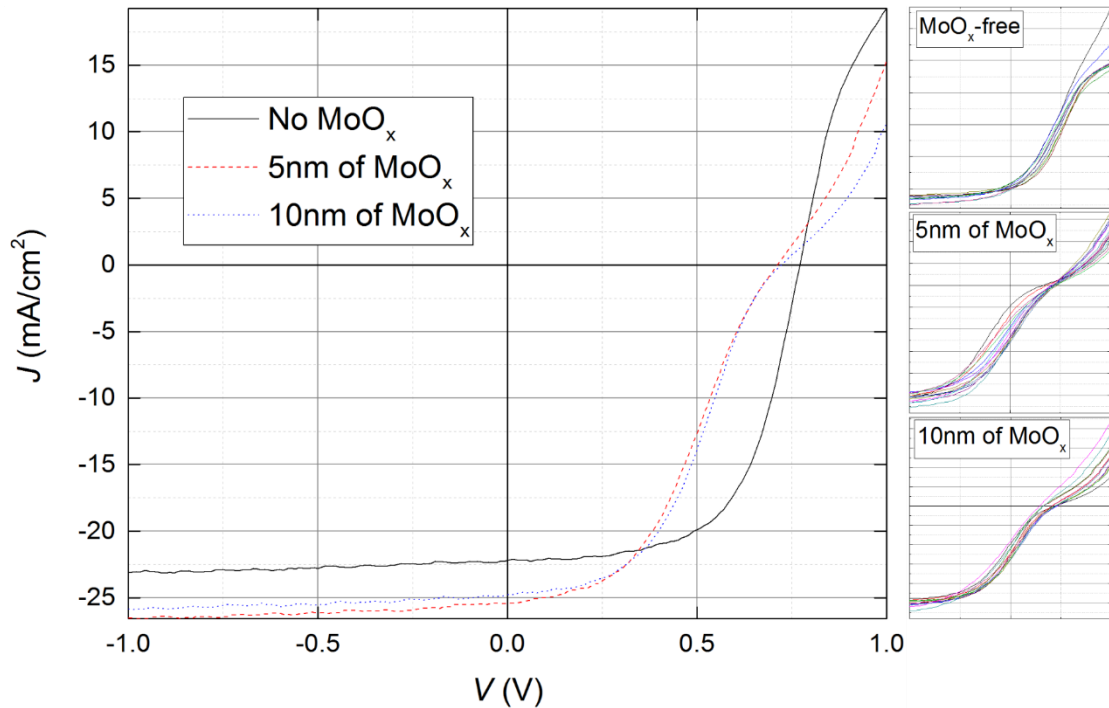
7.3.4.2 Study of the MoO_x /Au back contact behaviour of planar CdTe/CdS solar cells

Thermally evaporated MoO_x /Au back contact layers were studied as an alternative to Cu/Au. In Fig. 7.18, J - V curves of the best and all measured contacts are shown. Notably, incorporation of MoO_x layers on the back surface of the devices has a detrimental effect on the overall PV performance. All PV parameters apart from J_{SC}

Table 7.10 Peak and averages efficiencies of samples incorporating MoO_x layers of different thicknesses.

Sample	MoO _x (nm)	Peak efficiency (%)	Avg. efficiency (%)
MoO _x 0	0	10.46	9.58
MoO _x 5	5	7.91	6.79
MoO _x 10	10	7.98	7.38

show reduced values with the *FF* having the biggest losses (Fig. 7.19). Similarly to the Cu-free devices of Section 7.3.4.1, MoO_x-free devices exhibit a ‘rollover’ effect in the 1st quadrant (high forward bias) due to non-ohmic back contact behaviour. Further evaluation of the distorted *J-V* curves of the MoO_x devices shows that the low *FF* is caused by inflection points (S-kinks) close to the *V*_{OC}. Such *J-V* curve kinks are often reported for organic photovoltaic devices and are usually attributed to material interfaces with misaligned work functions, carrier extraction¹⁸ and injection barriers¹⁹, charge accumulation²⁰, low conductivity/ high *R*_S values²¹, thickness/morphology effects of individual layers²² or reduced/imbalanced carrier mobilities^{23,24}. In our


 Fig. 7.18 *J-V* curves of planar devices with and without MoO_x layers. Left: highest efficiency contacts. Right: all measured contacts (only the 0 – 1 V range is shown)

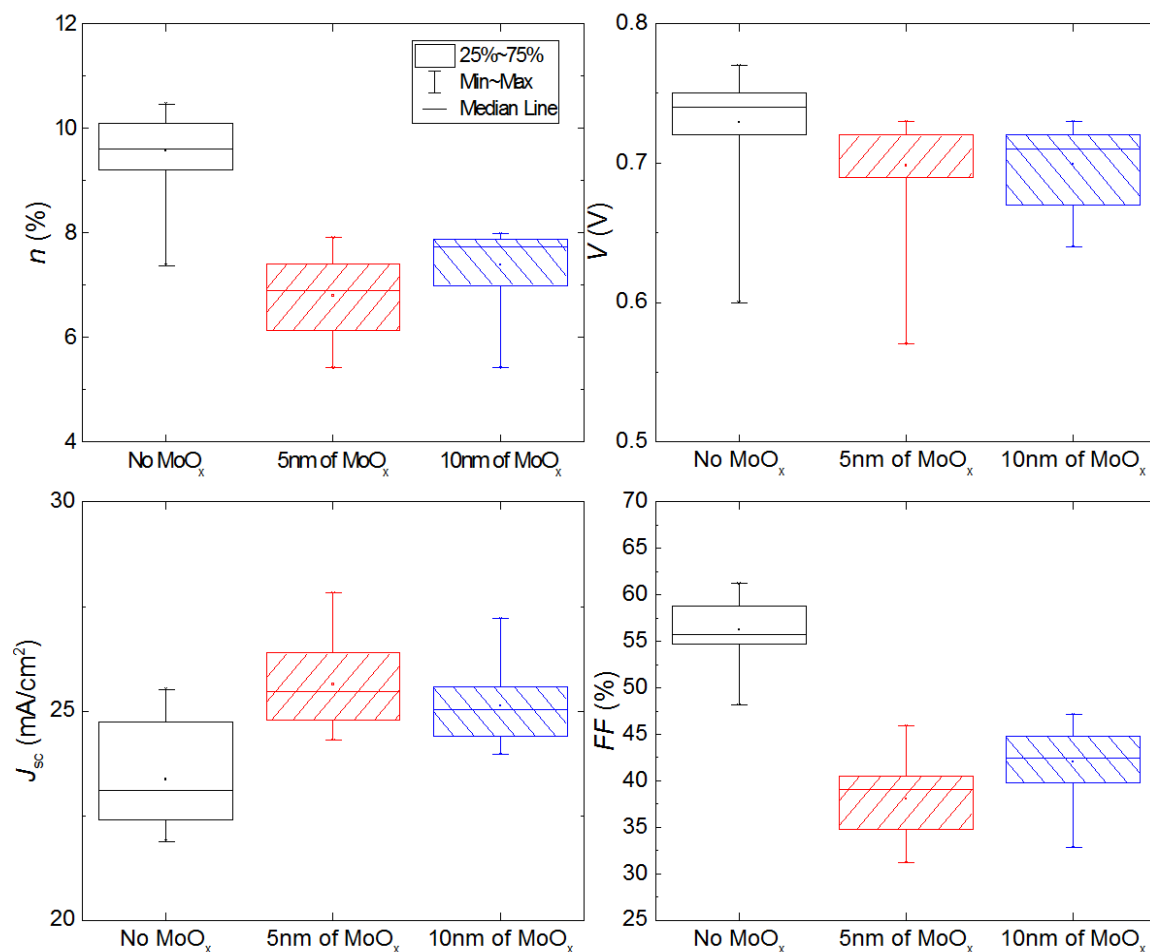


Fig. 7.19 Statistical analysis of the PV parameters η , V_{oc} , J_{sc} , FF for devices with varying MoO_x back contact layer thickness. Sample size for each boxplot is $N = 14$

experiments, the most probable reason for the S-kink is an interfacial energy barrier between the CdTe and the MoO_x layers and/or reduced hole mobilities in the MoO_x layer, which limit the hole transport. Indeed, purely stoichiometric MoO₃²⁵ or amorphous MoO_x²⁶ have been reported to have such detrimental effects. Although these assumptions may be valid, additional work is required.

7.3.4.3 Test of P3HT as a shunt-blocking layer on planar CdTe/CdS solar cells

The hypothesis that P3HT layers can be employed as a void-filling layer to block shunting paths between the CdTe and the TCO layers was investigated. In Fig. 7.20, the J - V curves of the experimental devices (Table 7.11) are shown (best and all measured contacts). Similarly to Section 7.3.4.2 and the MoO_x devices, the P3HT devices exhibit

Table 7.11 Peak and average efficiencies and R_S values of CdTe/CdS planar devices incorporating P3HT layers of varying thickness. 25 – 75 μl of P3HT solutions were spin-coated on three of the four samples

Sample	P3HT (μl)	η_{max} (%)	η_{avg} (%)	R_S ($\Omega\cdot\text{cm}^2$)
P3HT0	0	6.87	5.97	9 ± 1
P3HT25	25	3.7	2.7	49 ± 30
P3HT50	50	4.16	1.91	100 ± 112
P3HT75	75	5	3.01	59 ± 71

comparable S-kinks near the V_{OC} values. However, in the case of the P3HT layers the curve distortions are more severe in the power quadrant (low forward bias) with average R_S values ($N=12$) equal to $49 \pm 30 \Omega\cdot\text{cm}^2$ for sample ‘P3HT25’, $100 \pm 112 \Omega\cdot\text{cm}^2$ for sample ‘P3HT50’, $59 \pm 71 \Omega\cdot\text{cm}^2$ for sample ‘P3HT75’, whilst sample ‘P3HT0’ demonstrated low series resistance of $9 \pm 1 \Omega\cdot\text{cm}^2$. Moreover, the individual PV parameters of all measured contacts (Fig. 7.21), reveal a different trend to the MoO_x devices. Contrary to the reduce in η , J_{SC} and FF , incorporation of P3HT layers led to an increase in the open-circuit voltage. This may be attributed to the shunt blocking

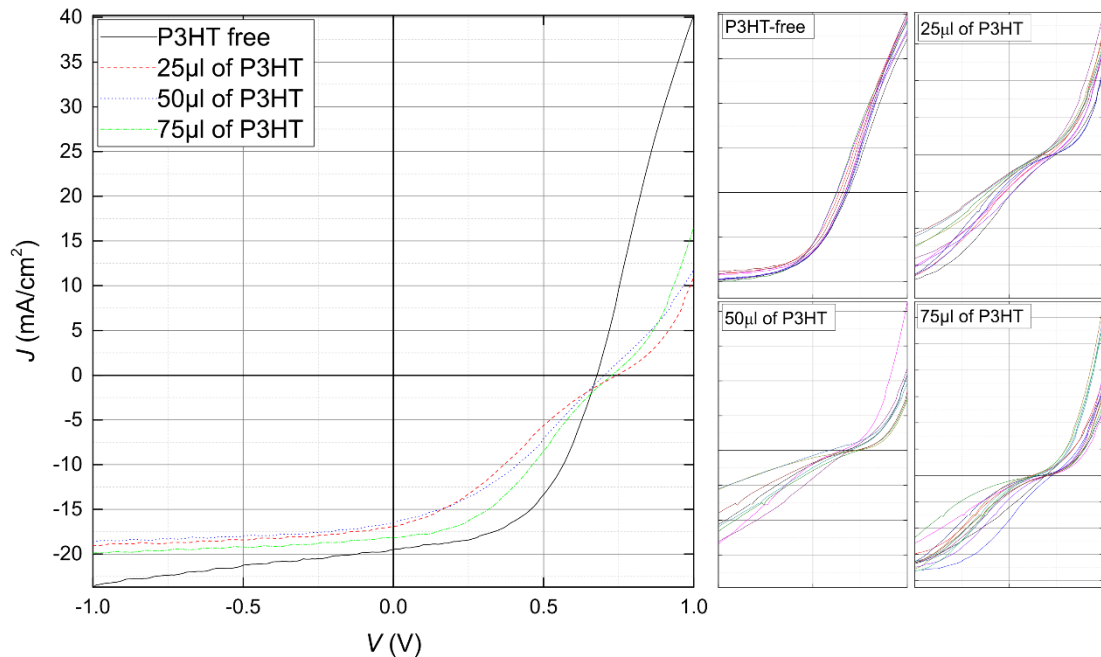


Fig. 7.20 J - V curves of planar devices incorporating 0, 25, 50 and 75 μl spin-coated P3HT layers. Left: highest efficiency contacts. Right: all measured contacts (0 – 1 V range)

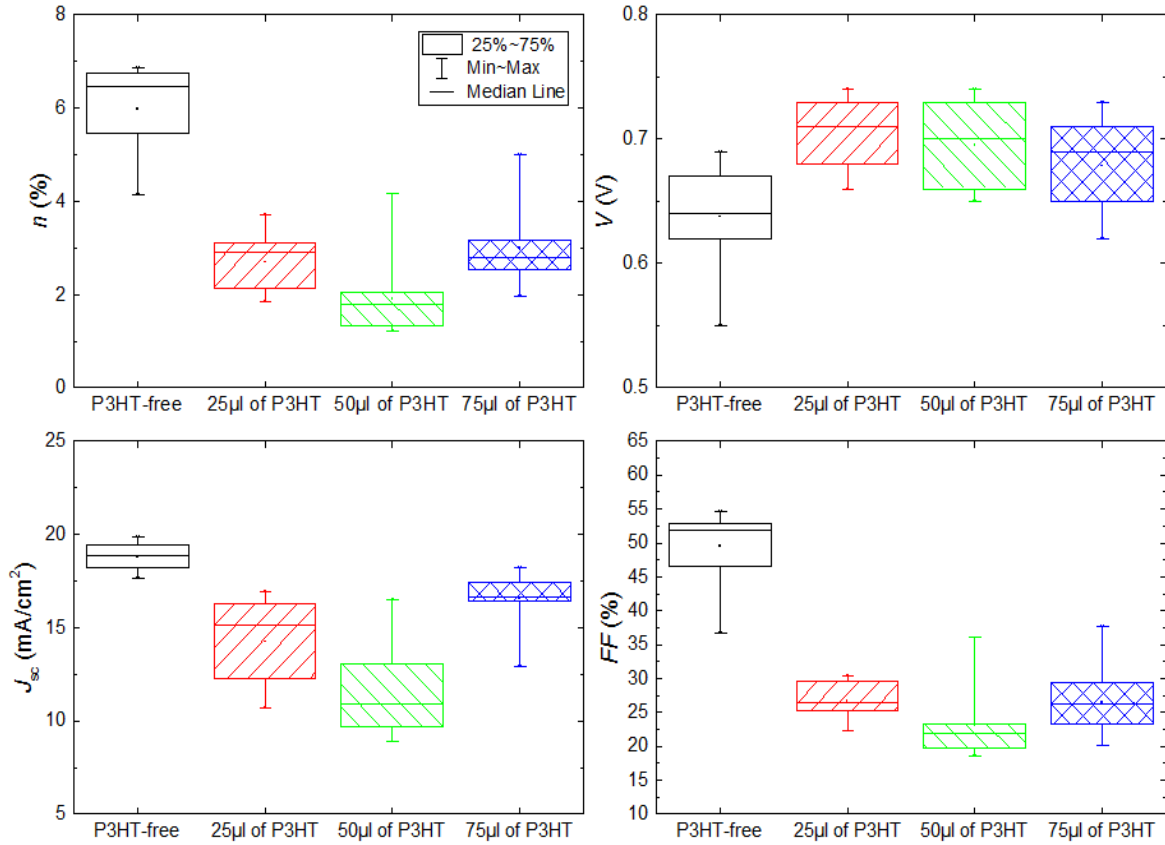


Fig. 7.21 Statistical analysis of the PV parameters η , V_{OC} , J_{SC} , FF for CdTe PV devices having P3HT/Au back contact layers of varied thickness. Sample size for each boxplot is $N = 12$.

properties of the P3HT layers or to artefacts due to the pronounced distortions in the J - V curves. Overall, J_{SC} and FF exhibit severe losses resulting in significant decrease of the power conversion efficiency. Similar assumptions to Section 7.3.4.2 can be made, addressing the S-kinks to mobility-related issues of the P3HT layer or CdTe/P3HT interfacial barriers.

7.3.5 Electrical characterisation of highest efficiency planar device

In this section light and dark J - V , EQE , temperature dependent J - V and C - V under dark conditions of the highest efficiency planar (TEC15/ZnO/CdS/CdTe/Cu/Au) PV device are presented. These series of measurements were performed to get a firm understanding of the planar device properties, so as to provide a control study for the microrod devices.

7.3.5.1 *J-V under dark and light conditions*

Fig. 7.22 shows the J - V curves under light and dark conditions. The performance parameters for the best contact are $\eta = 13.28\%$, $V_{OC} = 0.81$ V, $J_{SC} = 26.1$ mA/cm², $FF = 62.84\%$. Series and shunt resistances were extracted from the J - V curve with $R_S = 4.33$ Ω .cm² and $R_{SH} = 2076$ Ω .cm². The device's average PV parameters values ($N = 12$) are $\eta = 11.72 \pm 1.04\%$, $V_{OC} = 0.76 \pm 0.03$ V, $J_{SC} = 25.92 \pm 0.59$ mA/cm², $FF = 58.75 \pm 3.23\%$. Notably, regardless the layers' growth or MgCl₂ treatment conditions all devices exhibited non-uniform performance across the device area. As expected, the inclusion of the Cu back contact buffer layer resulted in 'rollover'-free J - V curves under high forward bias. However, the majority of the contacts demonstrate a 'crossover' between the light and dark J - V curves, as is often seen in CdTe/CdS solar cells. Comparison of these results with that from state of the art devices is deferred until Section 7.3.6.6.

7.3.5.2 *J-V-T under dark conditions*

J - V - T measurements in the 250-300 K regime were performed to explore the junction's electrical current transport mechanisms and to determine the back contact barrier height,

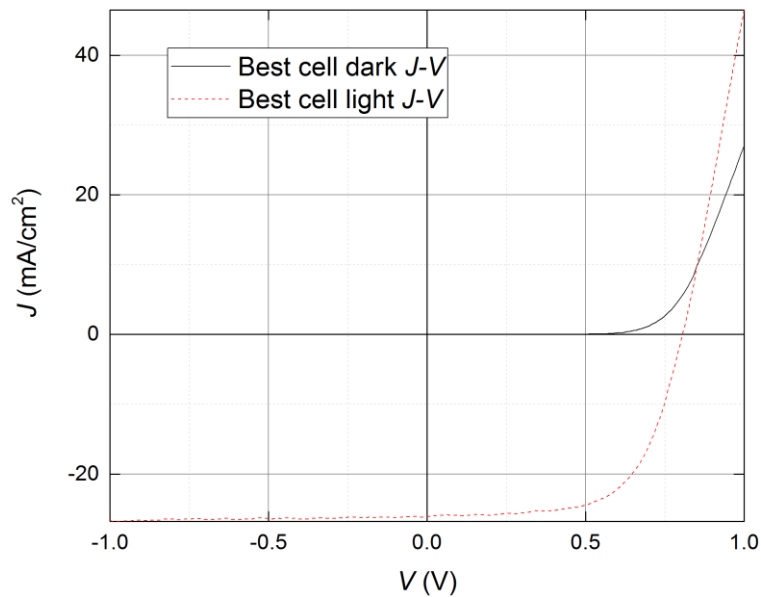


Fig. 7.22 J - V curves under light and dark conditions of the highest efficiency planar cell with $\eta = 13.28\%$, $V_{OC} = 0.81$ V, $J_{SC} = 26.1$ mA/cm², $FF = 62.78\%$

Φ_B , of the planar devices. As mentioned in Section 2.2.3.2, the carrier transport limiting effects can be investigated by analysing the temperature dependence of the ideality factor, n , and the reverse saturation current J_0 using the slope method. Although n only has a physical meaning only for values in the range $1 \leq n \leq 2$ and cannot be used to describe the physics of carrier transport mechanisms such as the multi-step tunnelling, its temperature relation was used to identify the type of the transport mechanisms as is usual in this field²⁸. In Fig. 7.23, $\ln J$ vs V plots of the data are shown – there are three distinctive regions. In Region I, since the forward bias values are smaller than the junction's turn-on voltage⁵, the current increases slowly with a non-exponential current-voltage response and, thus, the slope method of analysing the transport behaviour cannot be applied. Similarly, in Region III a non-exponential current-voltage response

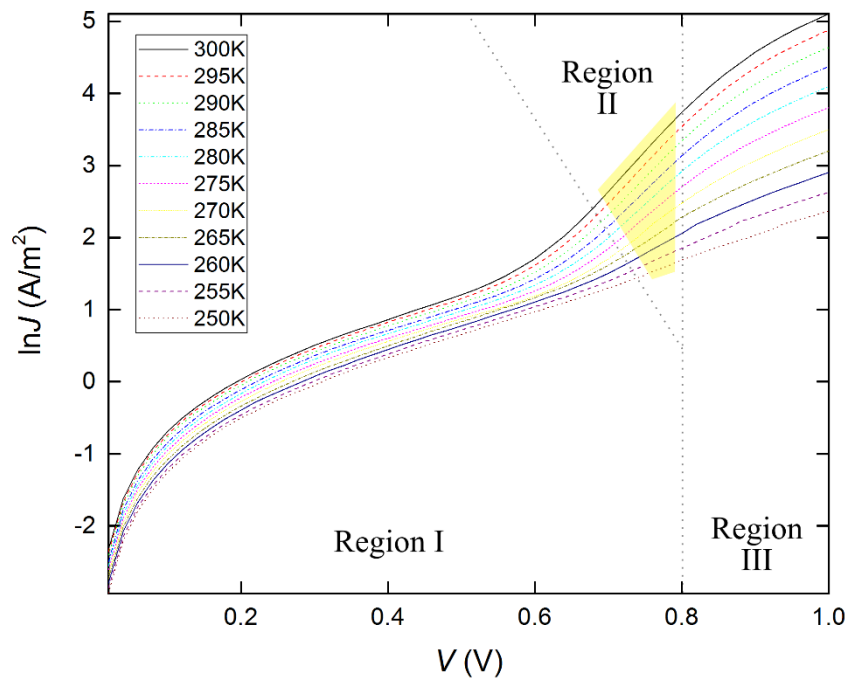


Fig. 7.23 J - V - T analysis of the highest performing planar CdTe/CdS solar cell: temperature dependent $\ln J$ vs V plot at forward bias demonstrating the low-bias (I), the linear response (II) and the high-bias regions (III)

⁵ The diode $V_{\text{turn-on}}$ is the threshold voltage, where diode rectification starts and current increases exponentially. Usually, $V_{\text{turn-on}}$ shifts to higher values with decreasing temperature.

can be observed. Generally, the current in this region is limited by the series resistance and the back contact ‘rollover’ effect if present, although the contribution from the ‘rollover’ effect for these samples is negligible. On the contrary the data in Region II was amenable to linear fitting. The extracted n and J_0 values were plotted against temperature and shown in Fig. 7.24a.

Evaluation of the $n - T$ and $J_0 - T$ plots shows a linear dependence of both the ideality factor and the saturation current to temperature, $n \propto T$ and $J_0 \propto T$. This linear response is relatively shallow in the 270 – 300 K regime and becomes steeper for temperatures below 270 K. By comparison with the literature reports, these findings indicate a multi-step tunnelling mechanism operating in the junction.

The number of tunnelling steps, R , that are required for the tunnelling process can be obtained from Eq. 2.12 (Section 2.2.3.2). For this calculation, the following values were used: $\epsilon_{\text{CdTe}} = 10.36 \epsilon_0$, $m_n = 0.1 m_e$ ²⁷. A CdTe doping density of $7 \times 10^{13} \text{ cm}^{-3}$ was estimated from C - V measurements presented in Section 7.3.5.4. The average number of tunnelling steps at 300 K were 1338 ± 17 . These values are an order of magnitude higher as compared to CSS grown superstrate devices found in the literature^{28,29}.

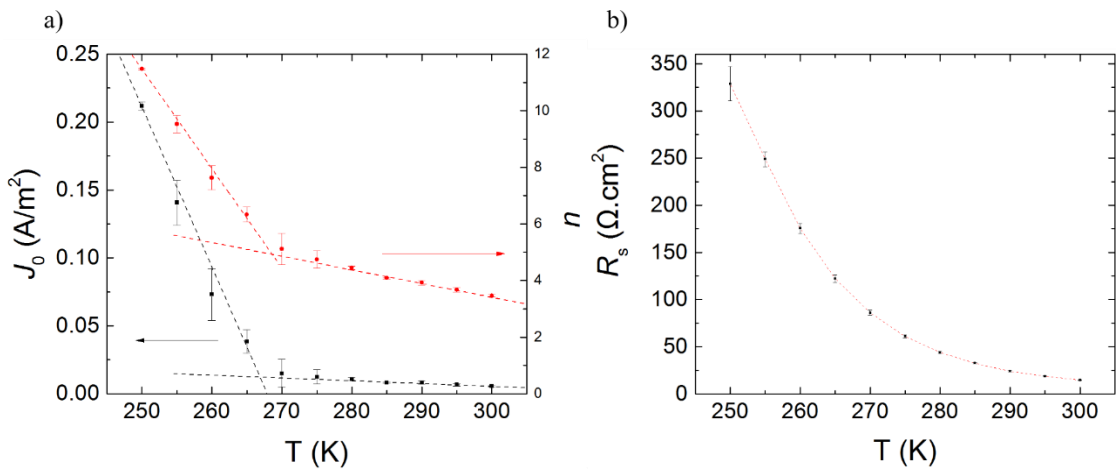


Fig. 7.24 J - V - T extracted a) ideality factor, n , and saturation current, J_0 , values plotted against temperature, b) plot of R_s against temperature used for the back-contact barrier height determination

For the calculation of the CdTe back contact barrier height, Φ_B , the method of Bätzner³⁰ was employed (Section 4.4.2). In Fig. 7.24b, temperature dependent R_S values were calculated from the slope of dark J - V curves and plotted against temperature. The barrier height was found to be 0.41 eV by fitting the extracted data to Eq. 4.9. Although this is slightly higher than that of similar devices reported elsewhere³, it appears to have had minimal impact on the solar cell performance. Indeed, according to other CdTe back contact studies^{31,32}, significant reduction of device performance is only observed when barrier heights exceed 0.5-0.6 eV.

7.3.5.3 EQE

Fig. 7.25 shows the *EQE* response of the highest efficiency planar device with a near-rectangular shape. To investigate the *EQE* losses due to parasitic absorption, the spectrum is divided in five spectral regions (I – V) defined by the FTO, ZnO, CdS and CdTe absorption edges. Additional *EQE* losses may occur due to reflections in the various interfaces of the device.

In regions I and II (< 405 nm), high *EQE* losses of ~ 80% are observed due to parasitic absorption in the ZnO and FTO layers. ZnO and FTO are the front-most layers of the device stack and have bandgap energies of $E_{g, \text{ZnO}}, E_{g, \text{FTO}} > 3$ eV. Therefore, light entering the device that is absorbed in these layers before reaching the CdTe absorber layer does not contribute to the photocurrent.

The *EQE* response of region III (405 – 555 nm) exhibit losses of ~ 30% and is limited by photon absorption in the CdS layer. CdS is a very good absorber and has a bandgap energy of 2.42 eV. However, light absorption in the CdS layer is undesirable, since it does not contribute to the current generation. Thus, an abrupt cut-off in the *EQE* response may be expected around 512 nm, the absorption edge of CdS. Instead, a more

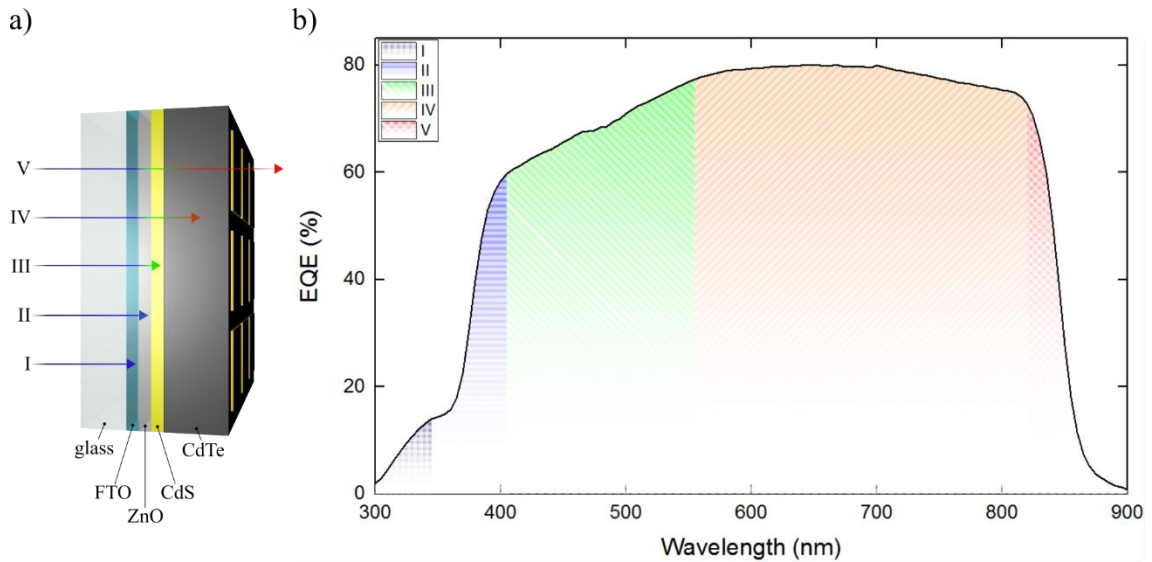


Fig. 7.25 a) Schematic diagram depicting the incident light penetration/absorption for the five *EQE* spectral regions. b) *EQE* response of the highest efficiency planar device ($\eta = 13.28\%$). The *EQE* curve is divided in five spectral regions based on the FTO, ZnO, CdS and CdTe absorption edges (boundaries between I – V)

gradual slope is observed. This behaviour can be explained by intermixing effects between the CdS and CdTe layers³³. Te diffuses from the CdTe into the CdS layer to form $\text{CdS}_{1-x}\text{Te}_x$ alloyed layer. The Te content in the intermixing layer lowers the bandgap energy of CdS creating a graded bandgap and shifting the p-n junction away from the metallurgical interface.

In the 555 – 825 nm range (region IV), the *EQE* curve appears relatively flat with average values of 78% (peaking at 80%). The small losses that appear for wavelengths above 700 nm are probably due to the CdTe layer being thin enough that incident photons escape the device without being absorbed³⁴. Photons – material interactions inside the device can lower the photon kinetic energy below the bandgap energy of CdTe leading to reduced light absorption. Additionally, low carrier lifetime may contribute to such losses³⁵.

The *EQE* response in region V ($\lambda > 825$ nm) is influenced by the bandgap of another intermixing layer. In the same way that Te diffuses into the CdS layer, S diffuses into

the CdTe layer to form a $\text{CdTe}_{1-y}\text{S}_y$ layer³⁶. The degree of intermixing lowers the CdTe bandgap (1.5 eV) and shifts the absorption edge to higher wavelengths.

7.3.5.4 C-V under dark conditions

C-V measurements under dark were performed in order to determine the doping density profile of the planar CdTe/CdS devices. The doping density and depletion region width values were extracted using the method described in Section 4.4.3. The results are presented in Fig. 7.26. A characteristic U-shape, often encountered in CdTe thin film solar cells is observed. However, interpretation of the C-V device characteristics and estimation of the carrier density can be problematic. For this reason, the C-V extracted carrier density and bias voltage were plotted against the normalised depletion region width (Fig. 7.27). The characteristics of the U-shaped curve is discussed further in Section 7.3.6.5. The average doping density was estimated from the minimum values of the measured U-shaped curves at $7 \times 10^{13} \text{ cm}^{-3}$, this being slightly lower than that of similar devices reported elsewhere^{3,37,38}.

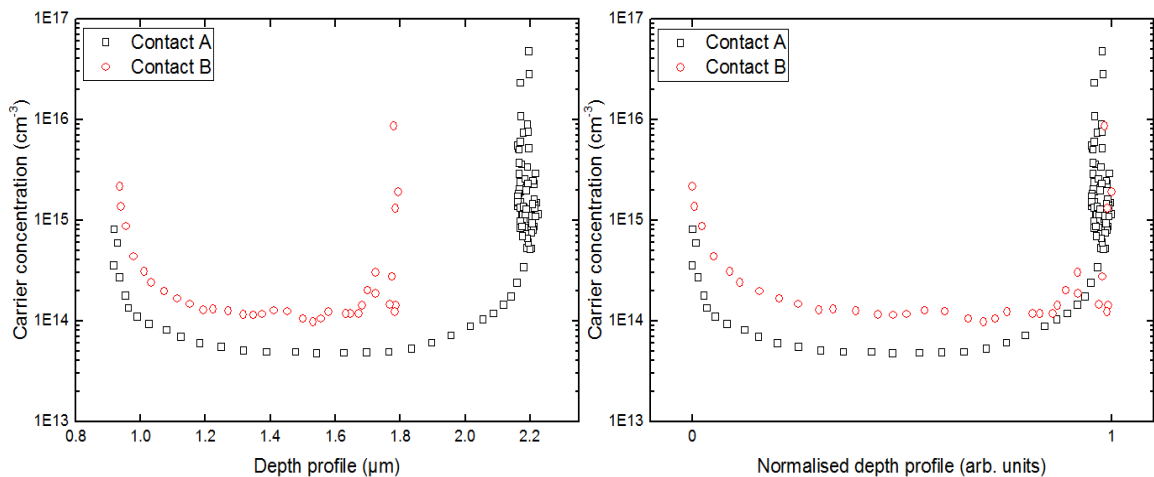


Fig. 7.26 C-V extracted carrier profile values: hole density versus depletion region width (left) and normalised depletion region width (right) plots of two contacts from the highest efficiency planar CdTe/CdS device ($\eta = 13.28\%$). The two plots depict the variations in depth profile and carrier concentration values observed across the total of the measured contacts. The normalised depth profile extends from 0 (CdTe/CdS interface) to 1 (near-back surface area)

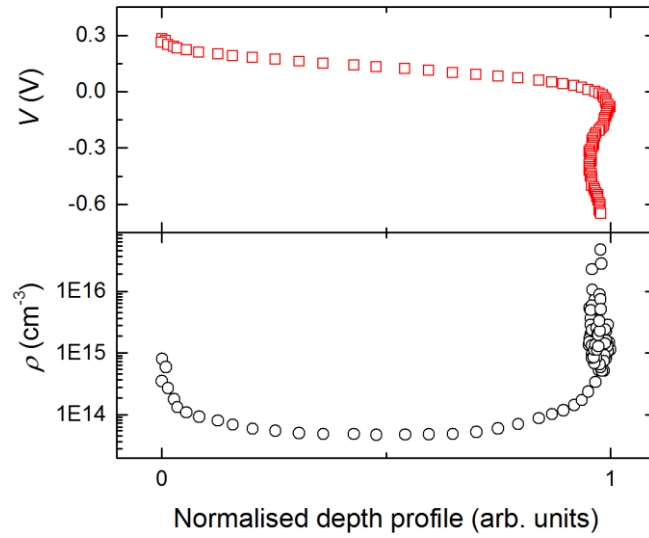


Fig. 7.27 C-V extracted carrier profile values: hole density (bottom) and bias voltage (top) versus depletion region width plots of the highest efficiency planar CdTe/CdS device ($\eta = 13.28\%$). The back-contact barrier height was ~ 0.4 eV using the method of Bätzner. The normalised depth profile extends from 0 (CdTe/CdS interface) to 1 (near-back surface area)

7.3.6 Discussion of planar device properties

7.3.6.1 Layer thickness optimisation of the planar CdTe/CdS device stack

The development of high efficiency planar CdTe/CdS solar cells with power conversion efficiencies peaking at $\sim 13\%$ required the optimisation of the individual layers, in particular the CdS (Section 7.3.1) and the CdTe (Section 7.3.2). The PV performance of all samples used in this chapter demonstrated a noticeable non-uniformity, which is related to the MgCl_2 process geometry. The key findings of these studies are discussed here.

In Section 7.3.1, the optimal CdS layer thickness was found to be 45 nm. The PV performance behaviour analysis of samples with thinner and thicker CdS layers, samples ‘CdS35’ (35 nm) and ‘CdS90’ (90 nm), revealed two counteracting mechanisms. Samples with a 90 nm thick CdS layer demonstrated severe J_{SC} losses especially for $\lambda < 500$ nm, while samples with a 35 nm thick CdS layer showed low V_{OC} and FF values; CdS is a good absorber with high absorption coefficient ($10^4 - 10^5 \text{ cm}^{-1}$

¹⁾³⁹. Therefore, a significant amount of incident photons with wavelengths below the CdS absorption edge, ~ 500 nm, are absorbed in the CdS layer. However, due to the low CdS hole lifetime, the $e - h^+$ pairs that are generated near the front surface of the device recombine fast before reaching the PV junction. Thus, thinning of the CdS layer from 90 to 45 nm resulted in higher *EQE* response below and above the CdS bandgap, while V_{OC} and *FF* values did not show any significant changes. This increase in the spectral response can be explained by reduced parasitic absorption in the CdS layer. However, further thinning of the CdS layer to 35 nm (sample ‘CdS35’), led to *EQE* losses and severe reduction in the V_{OC} and *FF* values. Thinning of the CdS layer below a critical thickness results in low film coverage and the formation of discontinuities in the CdS layer. Such discontinuities act as shunting paths between the CdTe and the FTO layers resulting in significant deterioration of the junction quality and V_{OC} and *FF* losses. Moreover, very thin CdS layers have been reported to influence the structural properties of CdTe/CdS solar cells with a negative impact on the formation of the $\text{CdS}_{1-x}\text{Te}_x$ intermixing layer and the crystallinity of the CdTe layer⁴⁰.

The effect of the CdTe layer thickness on the PV performance of planar CdTe/CdS devices as described in Section 7.3.2 can be summarised as follows. Decreasing CdTe thickness resulted in an overall decrease of all PV parameters, η , V_{OC} , J_{SC} , *FF*. In particular, comparison of average V_{OC} values of samples ‘CdTe16’ (1.6 μm) and ‘CdTe09’ (0.9 μm) showed a 20% decrease, while average *FF* values were reduced by 16%. This deterioration of the open circuit voltage and fill factor can be ascribed to shunting defects, such as pinholes in the CdTe layer. The extracted average R_{SH} values (Table 7.4), show a 4-fold decrease in 0.9 μm and 1.3 μm thick samples as compared to 1.6 μm ones. Conversely, R_S values increase marginally with thinning of the CdTe layer although thicker CdTe layers are expected to exhibit higher series resistance values.

Similar findings have been reported elsewhere^{41–43}. The losses in the J_{SC} were accompanied with a decrease in the EQE response with decreasing absorber layers. Numerical simulations⁴⁴ and previous reports⁴⁵ show an EQE deterioration towards low energies with decreasing CdTe thickness. Such spectral response was attributed to decreasing photon absorption for increasing wavelengths. Nevertheless, in this work, a uniform decrease in the EQE response was observed over the whole spectrum.

7.3.6.2 The $MgCl_2$ activation step and back surface analysis

Cl treatment of CdTe solar cells is a key manufacturing process which influences a) the doping of the CdTe thin film⁴⁶, b) formation of the p-n junction^{47,48}, c) grain boundary passivation⁴⁹, d) recrystallisation and grain growth^{50,51}. These effects have a beneficial impact on the overall PV performance of CdTe devices⁵². For this work, the novel $MgCl_2$ treatment process was employed and to the best of our knowledge this is the first report of its application on all-sputtered CdTe solar cells. Some of the $MgCl_2$ or $CdCl_2$ activation ‘recipes’ found in the literature include a dry or wet etching step before the Cl activation step. This etching process is reported to improve the Cl^- in-diffusion³⁸ and was found to be beneficial for the development of CSS grown devices in Chapter 6. Thus, prior to the activation step, sputtered planar CdTe/CdS samples were immersed in a N-P etching solution (70% H_3PO_4 , 29% H_2O , 1% HNO_3) for 2 to 15 seconds and the evolution of their PV performance was evaluated. The results show that this pre-treatment N-P etching step has detrimental effects on the PV performance of sputtered planar CdTe/CdS devices, since all demonstrated severe shunting and extremely low efficiencies. As-grown sputtered CdTe films (Fig. 7.7, Section 7.3.3.1) exhibit a high grain boundary density with gaps across the grain interfaces. Since the etching rate is often higher at the grain boundaries it is highly probable that voids and shunting paths are formed during the etching, which cause the deterioration of the PV performance. On

the contrary, CSS-grown CdTe films for PV applications are usually much thicker and more compact with larger grains and less grain boundaries.

Untreated planar CdTe/CdS devices demonstrated poor PV performance ($< 1\%$). As mentioned above, the grain structure of as-grown sputtered CdTe films revealed sub-micron grains with large gaps between them. There is therefore a high density of shunting pathways. Such grain characteristics are often encountered in CdTe sputtered films due to the low substrate temperatures used during the deposition. Usually, higher deposition temperatures generate films with a larger grain size⁵³. The reason for this is that at high temperatures the nucleation probability is lower and, therefore, grain growth dominates the formation of new grains⁵⁴. Moreover, according to the structure zone model⁵⁵, the grain structure of the deposited film is governed by the ratio T_s/T_m , where T_s is the substrate temperature and T_m is the melting point of the deposited material. It suggests that films generated at low T_s/T_m values have voided boundaries, fibrous nanograins and intrinsic stress. During the CdTe sputtering, a substrate temperature of 300°C was used, while the melting point of CdTe is 1092°C. The MgCl₂-induced grain growth and recrystallisation results in grains with sizes in the micron regime and the formation of a more compact film.

Evaluation of the Raman spectra of as-grown and MgCl₂ treated spectra reveal two main trends: a) a shift of the peaks/shoulders centres of the treated samples spectra to higher average frequencies by 1 to 4 cm⁻¹ and b) a decrease in the intensity of the spectral features for frequencies below 100 cm⁻¹ (low frequency tail) and above 150 cm⁻¹ (high frequency tail). At this point, it should be noted that the Te Raman scattering cross-section is at least two orders of magnitude higher than that of CdTe^{56,57}. Therefore, the peaks' size/area cannot be used for quantitative analysis. Nevertheless, the

wavenumbers of peaks from the treated samples and bulk values agree well. The observed Raman downshift in the untreated samples implies the occurrence of size- or stress-induced effects. This interpretation is consistent with reports that Cl/annealing treatments act to release the stress between the grains during the recrystallisation process^{58–62} and result in higher crystal quality films.

The features detected in the low and high frequency tails are probably related to elemental Te that at the grain boundaries, TeO₂ phases or surface/disorder-induced effects. During the deposition of CdTe polycrystalline films excess tellurium is known to segregate to the grain boundaries⁶³ forming crystalline Te inclusions. Such inclusions are known to act as carrier trap defects^{64,65}. Therefore, the intensity decrease of these features for the MgCl₂ treated samples can be related to a decreased grain boundary density as observed in the SEM micrographs. Overall, the Raman spectra of treated and untreated samples shows an improvement in the crystal quality of the treated samples in agreement with the SEM observations and the PV performance measurements. Such effects are probably due to stress relaxation in the grain structure, grain growth and recrystallisation and lower grain boundary density.

Post-MgCl₂ SEM/EDX analysis of the back surface show the existence of small amounts of Mg, Cl and O. However, due to the X-ray generation volume expanding hundreds of nanometres inside the CdTe layer, it is unclear in some cases whether these elements are located on the surface or diffused into the bulk of the device. Nevertheless, SEM micrographs show areas with evident surface impurities, which may account for performance deviations across the sample's contacts. Moreover, such impurities may have detrimental effects on the back-contact properties of the solar cell devices inducing

carrier extraction barriers, increased sheet resistance and may therefore act as a limiting factor in the PV performance.

7.3.6.3 *N-P and plasma etching after $MgCl_2$ treatment*

Conventionally, the fabrication of ‘superstrate’ CdTe/CdS solar cells involves the etching of the CdTe back surface with N-P acids, bromine/methanol or other etchants^{66,67}. It is found that prior to contacting such etching processes improve the back-contact properties by cleaning the back surface from residues/contaminations and by forming a p⁺-doped Te-rich layer at the back surface of the CdTe. The back-contact properties are further enhanced with the deposition of a thin Cu layer after the etching step. In this way, a Cu_xTe alloyed layer can be formed which is highly p-doped and reduces the ‘rollover’ effect often encountered in CdTe solar cell devices. However, in this work, both N-P and Ar⁺ plasma treatments caused severe PV performance deterioration effects.

The SEM micrographs of N-P etched samples (Fig. 7.12) showed that the film had been disrupted by the treatment and had begun to blister and crack. This suggests that the sputtered CdTe films are more sensitive to the N-P etching solution than the CSS ones, perhaps due to different strain, grain size and thickness (< 2 μm). As a result, a high density of shunting pathways was formed which resulted to poor shunting resistance values. This behaviour is consistent with pre-MgCl₂ N-P etching experiments (7.3.6.2) and etching experiments with microrod devices, where the whole layer stack delaminated even for very short etching time intervals. Although N-P etching had adverse effects generally, etching of samples for very short time intervals of 1 – 2 secs contributed to the decrease of the ‘rollover’ effect. However, these samples also demonstrated decreased R_{SH} values. Moreover, since sputtered CdTe layers are highly sensitive to the N-P etching, control over such short time intervals was problematic.

The J - V curves of samples that were plasma etched show a decrease in the R_{SH} values and pronounced S-kinks and ‘rollover’ effects. The SEM/EDX analysis showed wire-like structures on the CdTe surface with a high O and Cl content. Although the etching process was conducted in a pure Ar ambient, these impurities may come from the sputtering chamber where the plasma etching is performed. This same chamber is regularly used for the deposition of various oxides. Thus, oxygen contamination from the chamber during the plasma etching may react with the samples to form such irregularities. $MgCl_2$ process residues, as shown in Section 7.3.3.1 may add to the effect. Moreover, non-optimised plasma etching is reported to have adverse effects by forming a highly defective back contact layer⁶⁸. Overall, the J - V curve distortions can be ascribed to carrier extraction barriers or high R_S values due defects and impurities on the back surface of the device.

Conclusively, both N-P and plasma etching experiments resulted in reduced performance of the planar CdTe/CdS devices due to formation of defects and impurities. However, high performance unetched devices with efficiencies peaking at ~ 13% were fabricated. On the contrary, pre- and post- Cl activation etching steps are mandatory in order to fabricate CSS grown CdTe devices with similar efficiencies.

7.3.6.4 Back contacts

Three back contact configurations, Cu/Au, MoO_x /Au and P3HT/Au were investigated as alternatives to Au contacts. While the aim of the Cu, MoO_x layers incorporation was to improve the carrier extraction by lowering the back-contact barrier height, P3HT layers were tested as shunt-blocking layers.

The use and effects of Cu in CdTe/CdS PV devices are extensively explored and well documented^{69–74}. Incorporation of small amounts of Cu enhances the PV performance

by effectively doping the CdTe layer and reducing the back-contact barrier width. Nevertheless, since Cu is well known to be a fast diffuser, Cu advances via the grain boundaries to the p - n junction and to the front part of the device with detrimental effects on the PV performance. Such effects include Cu_{Cd} substitutional, Cu_i interstitial defects and related complexes, formation of shunting paths and recombination centres. In this work, the optimal Cu layer thickness was 5 nm. Generally, in CdTe solar cell devices, the CdTe back surface is etched before the deposition of the Cu layer. Thus, a Cu_xTe alloyed layer is formed which is highly p-type and contributes in the diminishing of the ‘rollover’ effect often encountered in CdTe solar cell devices. Nevertheless, etching experiments that were performed on the back surface of planar CdTe/CdS MgCl_2 treated solar cells showed reduced PV performance due to the formation of defects and impurities.

The use of MoO_x and P3HT layers in planar CdTe/CdS solar cells devices had detrimental effects on the PV performance. The vast majority of the contacts demonstrated distorted J - V curves with S-kinks in the first and fourth quadrants similar to those found in organic photovoltaic devices. It maybe speculated that the causes are interfacial energy barriers between the CdTe and the MoO_x /P3HT layers and/or reduced carrier mobilities in the MoO_x /P3HT layers. However, additional studies would be required to test this hypothesis.

7.3.6.5 Electrical characterisation of highest efficiency planar device

The highest efficiency planar CdTe/CdS device demonstrated peak performance parameters of $\eta = 13.28\%$, $V_{\text{OC}} = 0.81 \text{ V}$, $J_{\text{SC}} = 26.1 \text{ mA/cm}^2$ and $FF = 62.78\%$. Detailed information of the device configuration is given on Table 7.2 (Section 7.2.2). Notably, the very thin CdS and CdTe layers that were used, 45 nm and 1.8 μm in thickness respectively, imply a high-quality deposition process producing smooth, homogeneous

films. Usually, high efficiency devices have > 60 nm thick CdS layers and $2 - 2.3$ μm thick CdTe layers^{9,75,76} in order to form a high-quality junction and minimise the pinhole density. Furthermore, the fabrication process did not include any etching steps before or after the Cl activation which, usually, are mandatory for the enhancement of the PV performance of CdTe solar cells. This could be a potential advantage in large scale fabrication of sputtered CdTe/CdS cells from a financial point of view.

J-V measurements of the best contacts showed a ‘crossover’ between the light and dark curves. This ‘crossover’ effect is often seen in CdTe/CdS solar cells and is ascribed to changes in the photoconductivity of the CdS layer under light and dark conditions mainly. Nevertheless, such changes in the photoconductivity of CdS are considered to have a very small effect on the PV performance in general^{77–80}. Particularly, the V_{OC} and J_{SC} values of the best contact are among the highest reported for sputtered devices (comparison of the J_{SC} from the *J-V* curve and from integrating the *EQE* gave a difference of just 0.8 mA/cm^2 and to the measured J_{SC} may be said to be reliable).

In accordance with the J_{SC} values, *EQE* measurements showed high spectral response especially for wavelengths above 400 nm. The losses in the 300 – 400 nm region are due to parasitic absorption in the TCO and CdS front layers. These losses can be reduced partly with the substitution of CdS with amorphous CdS:O, which is reported to have a wider bandgap^{81,82}. An additional effect of the CdS:O layer is the reduced S and Te inter-diffusion which lead to the formation of low and high x compositions of $\text{CdS}_x\text{Te}_{1-x}$ respectively. As seen in Fig. 7.25 (Section 6.5.2), the bandgap energies of the alloyed layers are redshifted when compared to that of CdS and CdTe. Although the formation of low x $\text{CdS}_x\text{Te}_{1-x}$ may lead to beneficial light absorption below the CdTe bandgap,

absorption in the high x composition is undesirable because it does not contribute to the current collection.

The C - V carrier profiles, Fig. 7.26 (Section 7.3.5.4), show a characteristic U-shaped curve as is usual for CdTe/CdS solar cells. Interpretation of the C - V device characteristics or even estimation of the carrier density can be problematic. According to Li⁸³, the left branch of the curve is related to the forward bias regime while the right branch corresponds to the reverse bias regime (Fig. 7.27). In the forward bias regime, usually the back contact ‘rollover’ effect can contribute to the C - V response leading to a false (apparent) increase in the carrier density. Moreover, charge distribution at the CdTe/CdS interface, Te/S intermixing and Cu diffusion effects may lead to similar results. Measurement errors induced by high forward bias which are known to affect the C - V response can be ruled out since the measurements in this work were performed under < 0.5 V bias. Although some works attribute the right branch of the curve to non-uniform carrier density, Li stresses the importance of additional factors that influence the extracted carrier densities: contributions from the ‘punch-through’ effect and deep levels at high reverse bias. During the ‘punch-through’ effect the depletion region expands and, eventually, reaches the back contact for the case of thin absorbers (e.g. 2 μm). Thus, a sharp increase in the carrier density from $\sim 10^{13-14} \text{ cm}^{-3}$ (indicative of CdTe) to $\sim 10^{17} \text{ cm}^{-3}$ (indicative of CdS or TCO) is observed. Lastly, a high density of deep levels may contribute to a false increase both of the right branch and the bottom of the curve. Due to the band bending, deep levels located at the front of the depletion region become ionised and, thus, may contribute to the space charge region. At reverse bias, the deep-level contribution increases with increasing applied voltage, since there is a higher degree of band bending.

The J - V - T measurements analysis showed that the carrier transport is governed by a multi-tunnelling mechanism. These findings are in accordance with Al Turkestani²⁸, Al-Allak²⁹ and Gaewdang⁸⁴. On the contrary, Williams⁸⁵ and Treharne⁸⁶ report a mix of two different mechanisms: recombination in the depletion region at high temperatures and multi-step tunnelling at low temperatures. Particularly, Treharne reports the change in the transport mechanisms at 250 K and Williams at 270 K. In this work, a change in the linear response of $n \propto T$ and $J_0 \propto T$ is observed at 270 K. The average number of tunnelling steps at 300 K were 1338 ± 17 . These numbers are similar to Williams' findings and an order of magnitude higher than the Al Turkestani implying a higher interfacial defect density. Nevertheless, these findings on the carrier transport mechanisms suggest significant changes in the PV performance at low temperatures only and are not expected to have any implications for room temperature operation.

7.3.6.6 Comparison of highest efficiency planar device to record efficiency all-sputtered CdTe/CdS devices

The up-to-date record efficiency of all-sputtered CdTe/CdS solar cells is 14.5% with $V_{OC} = 0.847$ V, $J_{SC} = 24.4$ mA/cm² and $FF = 69.8\%$ ⁹. Table 7.12 shows a comparison of the top three higher efficiency all-sputtered planar CdTe/CdS solar cells to the best cell in this work. The device in this work have a) similar V_{OC} (> 800 mV), b) higher J_{SC} and c) lower FF values than the record efficiency devices. Interestingly, Paudel's experiments with various Cl activation temperatures showed that devices treated at temperatures above 400°C demonstrated good J_{SC} values, but relatively lower V_{OC} , FF values due to stronger S diffusion and micro-structural changes during the activation step.

Although the V_{OC} of the best cell in this work is above 800 mV and comparable to Li's⁷⁵ and Gupta's⁷⁶, it is slightly lower than the one reported by Paudel. One factor that can

Table 7.12 Comparison of the record all-sputtered planar CdTe/CdS solar cells to the highest efficiency cell of this work: CdS, CdTe layer thickness, back contact area and PV performance parameters

Lab	CdS (nm)	CdTe (μm)	Contact (cm^2)	η (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
Paudel	55 – 60*	2.1	0.08	14.5	847	24.4	69.8
Li	100*	2-2.3	0.07	14.4	804	24.8	72.4
Gupta	130	2.3	NA	14	814	23.6	73.2
This work	45	1.8	0.12	13.3	810	26.1	62.8

*amorphous CdS:O window layer was used instead of CdS

affect the formation of a high-quality junction is the window layer thickness. As discussed in Section 7.3.6.1, devices with thin CdS may suffer from low V_{OC} values due to high density of pinholes in the CdS/CdTe interface. Furthermore, the CdS layer thickness decreases even more during the MgCl_2 treatment, because of the inter-diffusion of S and the formation of the Te-rich $\text{CdS}_x\text{Te}_{1-x}$ alloyed layer. In this work, a very thin CdS layer (45 nm) was used in order to maximise the current collection, while the devices presented in Table 7.12 have either much thicker window layers or an amorphous CdS:O instead of CdS layer. As discussed in Section 7.3.6.5, CdS:O layers limit the inter-diffusion of Te and the consumption of the CdS layer during the Cl treatment process. Markedly, Paudel achieved an efficiency increase of $\sim 1\%$ over their previous record device with $\eta = 13.6\%$, $V_{OC} = 0.831$ V, $J_{SC} = 22.7$ mA/cm^2 and $FF = 72.2\%$ (0.12 cm^2 contact area) by substituting the previously used 80 nm thick CdS layer with a 55 – 60 nm thick CdS:O layer. In this way, higher J_{SC} values were achieved while retaining high V_{OC} values.

A second factor that may result in lower V_{OC} values is the thickness of the CdTe layer (1.8 μm) in this work, this being the thinnest when compared to the other three devices. The reasons can be either a high density of shunting paths or insufficient photon absorption due to the finite thickness of the CdTe layer. Nevertheless, devices with

CdTe layers up to 2 μm were fabricated in this work, but demonstrated lower power conversion efficiencies perhaps due to non-optimised Cl activation.

A third factor that influences the PV performance is the contact area. In this work, a 0.12 cm^2 contact area was used, which was much larger than the comparison devices. Due to the polycrystallinity of the CdS and CdTe layers, fluctuations in the shunting paths density and the junction quality across the CdTe/CdS interface exist. Such variations have a strong effect on the PV performance and become more evident with increasing contact area.

Lastly, commercial glass substrates may have different optical properties (transmittance, haze), FTO sheet resistance values or may limit the impurities diffusion from the substrate to the junction by incorporating blocking layers. In this work, Pilkington NSG TEC C15M glass substrates were used, while Paudel, Li and Gupta used high quality low-iron soda-lime glass (SLG) or aluminosilicate substrates with unknown specifications. Therefore, a comparison of the substrate impact on the PV performance between this and Paudel's, Li's and Gupta's work cannot be established.

In order to interpret the high J_{SC} values, a qualitative comparison of the *EQE* response of the best cell in this work and Paudel's best cell has been conducted by comparing the area beneath the *EQE* curves. The comparison shows an approximately 8% higher current collection in Paudel's work. Specifically, the *EQE* response of Paudel's cell exhibited ~ 50% gain in the 300 – 345 nm range (region I), ~ 30% gain in the 345 – 405 nm (region II), ~ 1% gain in the 405 – 555 nm (region III), ~ 10% gain in the 555 – 825 nm (region IV) and ~ 25% decline in the 825 – 900 nm (region V). In regions I, II, III and V the changes in the *EQE* response can be ascribed to the higher transmittance of the thin CdS:O window layer and the reduced Te/S inter-diffusion. Moreover, the use

of high quality $\text{SnO}_2\text{:F/SnO}_2$ low iron SLG substrates may have an extra contribution in regions I and II due to the lower absorption in the SnO_2 HRT layer when compared to ZnO that was used in this work. Lastly, the higher EQE values of region IV can be ascribed to the thicker CdTe layer that was used in Paudel's work or else to enhanced carrier lifetimes. Although these findings are in accordance with the discussion made in the previous paragraphs, comparison of the EQE curves of the two cells reveals inconsistency with the J_{SC} values in Table 7.12 from J-V measurements. Therefore, we conclude that one or both of Paudel's and this work's data is subject to errors in the solar simulator calibration, area measurement or the EQE measurement.

The best planar CdTe/CdS reported in this work demonstrated low FF values relative to the comparison devices, as shown in Table 7.12. Since the fill factor is a measurement of the J - V curve 'squareness', a comparison of the R_S and R_{SH} values of this and Paudel's work has been performed. Paudel reports $R_S = 4.1 \text{ } \Omega\cdot\text{cm}^2$ and $R_{SH} = 1010 \text{ } \Omega\cdot\text{cm}^2$, while for this work the resistances were calculated as $R_S = 4.3 \text{ } \Omega\cdot\text{cm}^2$ and $R_{SH} = 2076 \text{ } \Omega\cdot\text{cm}^2$. It should be noted that the R_S values were extracted from the inverse of the slope near the V_{OC} , while the R_{SH} near J_{SC} . The device of this work has similar series and higher shunt resistance than Paudel's, which suggest higher FF values. In practise, however, the fill factor in this work is 10% lower. Since the effects of R_S and R_{SH} have been investigated, the losses in the FF are probably due to an overall lower junction quality. Indeed, the EQE , J - V - T and J - V measurements showed a) thicker intermixing layers, b) the existence of a trap assisted multistep tunnelling mechanism at the space charge region and c) the presence of photoconductive effects in the CdS layer ('crossover' effect). Such phenomena may result in low turn-on voltage and low FF values in return, which are encountered in this work.

7.4 CdTe/CdS solar cell devices developed on ZnO microrod coated substrates

7.4.1 SEM/EDX investigation of the CdTe/CdS microrod devices development

A description of the samples studied by SEM/EDX is given in Table 7.13– this set was chosen to investigate the sequential effects of overgrowth and processing required to build up full devices.

Fig. 7.28a shows an SEM secondary electron plan view micrograph of a sample containing as-grown ZnO microrods, while Fig. 7.28b shows the cross section of the same sample (sample ‘SEM1’). The average microrod areal density was $\sim 10^4 \text{ cm}^{-2}$, the average diameter $\sim 450 \text{ nm}$ and the average microrod length ranged from 1 to 2 μm approximately. The layer beneath the microrods, as marked in Fig. 7.28b, is the FTO layer (400 nm).

In Fig. 7.28c and d, 40° angle view micrographs of samples ‘SEM2’ and ‘SEM3’ demonstrate the coating of the ZnO microrods with the CdS and CdTe layers. Notably, both flat areas of CdTe continuous film and CdTe ‘hillocks’ can be observed in sample ‘SEM3’. The ‘hillocks’ indicate the positions of coated ZnO microrods, while the flat areas are planar parts of the sputtered CdTe film.

Table 7.13 Description of the samples used for the SEM/EDX characterisation of the microrod CdTe/CdS devices during the various stages of the fabrication process

Sample ID	Description	CdS (nm)	CdTe (nm)
SEM1	As-grown ZnO microrods	-	-
SEM2	CdS coated ZnO microrods	180	-
SEM3	CdS/CdTe coated ZnO microrods	180	2000
SEM4	MgCl ₂ treated microrod device	180	2000

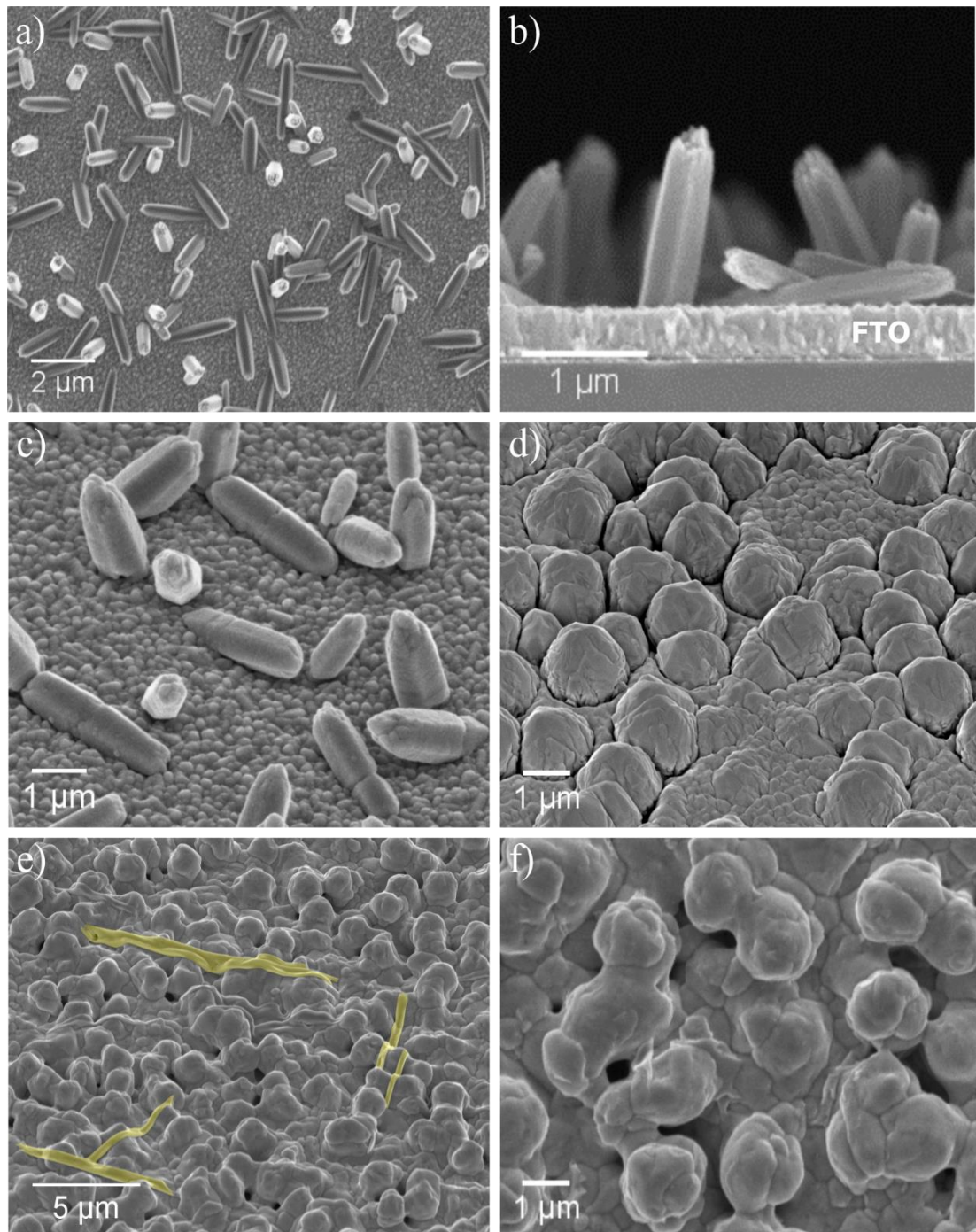


Fig. 7.28 a) Top and b) cross-sectional views of as-deposited ZnO microrods grown on TEC/FTO substrates (sample 'SEM1'). c) 40° angle view of CdS (sample 'SEM2') and d) CdTe/CdS coated ZnO microrods (sample 'SEM3'). Areas of continuous CdTe film and CdTe 'hillocks' can be observed indicating the position of coated ZnO microrods. e) 40° angle and f) top views of the back surface of a MgCl_2 treated microrod device (sample 'SEM4'). Voids and ribbon-like structures (marked in yellow) are evident

The standard MgCl_2 activation step at 420°C (20 mins) was performed on sample ‘SEM4’ after the CdTe layer deposition. In Fig. 7.28e and f, SEM micrographs of the back, i.e. the CdTe, surface of the device are presented. A comparison of the surface morphology before and after the high temperature MgCl_2 treatment show a) the smearing of the CdTe ‘hillocks’ and their fusion with the film, b) the development of numerous voids with diameters that range from few nanometres to $1 - 2 \mu\text{m}$ and c) the formation of ribbon-like surface structures. In Fig. 7.29, cross-sectional SEM micrographs of the MgCl_2 treated device are shown. Notably, some of the surface fissures extend further inside the CdTe layer as shown in Fig. 7.29a. Moreover, additional voids near the ZnO microrods and discontinuities in the CdS layer are observed. Apparently, changes in the crystal structure of the CdTe film are induced during the Cl activation step due to recrystallisation effects as discussed in Section 7.3.6.2.

The chemical composition of the surface features, i.e. the voids, ‘hillocks’ and ribbon-like structures were studied by means of SEM/EDX analysis. The elemental analysis of

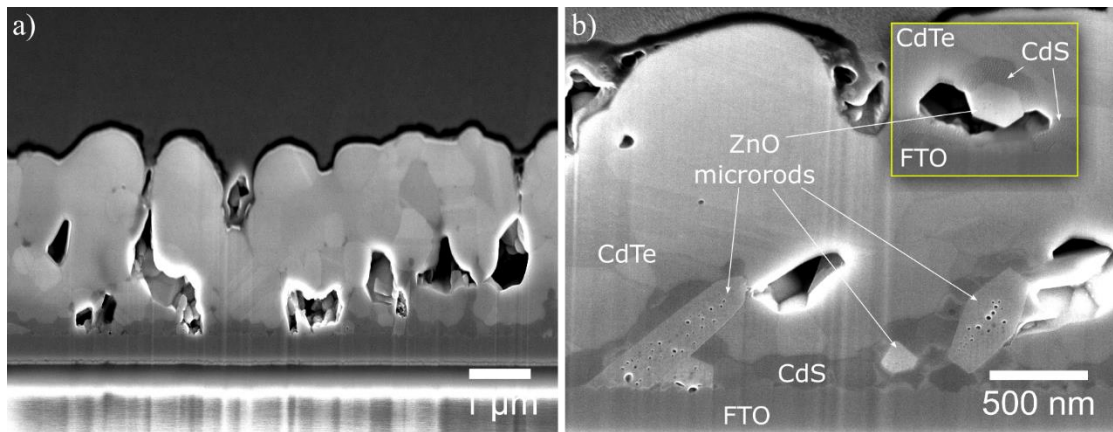
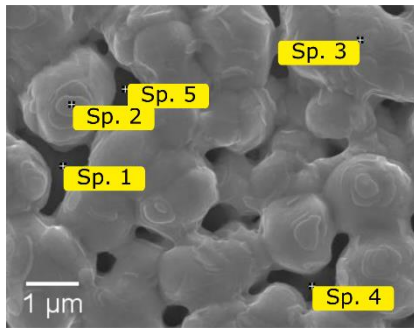


Fig. 7.29 SEM cross-sectional views of a MgCl_2 treated microrod device (sample ‘SEM4’). Defects, such as fissures that extend deep inside the absorber layer (a) and discontinuities in the CdS layer plus voids close to the ZnO microrods (b) are evident. Inset: image showing a ZnO microrod (hexagonal cross-section), partly coated with a CdS layer and a void formed beneath.

Table 7.14 elemental analysis of spectrums Sp. 1-5



Spectrum	O (at.%)	Cl (at.%)	Cd (at.%)	Te (at.%)
Sp. 1	0	0.3	52	48
Sp. 2	0	0.54	52	47
Sp. 3	0	0	52	48
Sp. 4	7.55	1.34	47	45
Sp. 5	0.89	0.3	50	49

Fig. 7.30 secondary electron SEM micrograph showing the sites used for the EDX analysis of the MgCl_2 treated microrod devices.

the ribbon-like structures did not show any difference from the bulk and, thus, it is not presented here. It is highly probable, that the signal coming from such thin surface features is not detectable due to the large X-ray generation volume; the penetration depth of the primary electron beam is estimated close to $1\ \mu\text{m}$. The EDX analysis results of the other surface features are presented in Table 7.14 with the points used for the data acquisition being shown in Fig. 7.30. In common with the analysis of the back-surface of treated planar devices, areas with varying O and Cl concentrations were observed. Such impurities are most likely to be residues from the activation process.

7.4.2 Electrical characterisation of highest efficiency microrod device

7.4.2.1 J-V under dark and light conditions

Fig. 7.31 shows the J - V curves of the highest efficiency microrod device obtained under light and dark conditions. The corresponding performance parameters for the best contact are $\eta = 6.18\%$, $V_{OC} = 0.62\ \text{V}$, $J_{SC} = 22.56\ \text{mA}/\text{cm}^2$ and $FF = 44.16\%$. However, extreme variations in the performance between individual contacts were observed. The device's average PV parameters values ($N = 12$) are $\eta = 2.8 \pm 1.78\%$, $V_{OC} = 0.52 \pm 0.06\ \text{V}$, $J_{SC} = 15.89 \pm 4.55\ \text{mA}/\text{cm}^2$ and $FF = 30.42 \pm 7.69\%$. Such large variations in performance are ascribed to a non-homogeneous MgCl_2 treatment. In Fig. 7.32, these

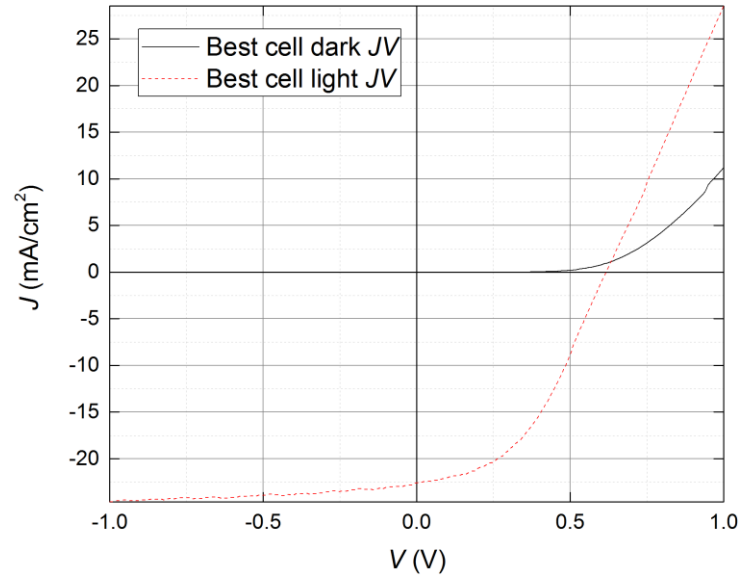


Fig. 7.31 J - V curves under light and dark conditions of the highest efficiency microrod cell with $\eta = 6.18\%$, $V_{OC} = 0.62$ V, $J_{SC} = 22.56$ mA/cm², $FF = 44.16\%$

performance variations are visualised using contour maps of the extracted η , V_{OC} , J_{SC} and FF values. Although the microrod devices were treated in the exact same way as the planar devices, the $MgCl_2$ vapour and Cl diffusion appears to be problematic. Treatment of the microrod devices for longer time intervals resulted in lower PV performance. An additional contribution to the performance variations is the fissures density across the device area. The series and shunt resistances values were extracted from the J - V curve and were $R_S = 14.2$ $\Omega \cdot \text{cm}^2$ and $R_{SH} = 190$ $\Omega \cdot \text{cm}^2$. The measured device did not show any ‘rollover’ effect due to the employment of a Cu/Au back contact layer stack. However, most of the contacts demonstrated pronounced ‘crossover’ between the light and dark J - V curves.

7.4.2.2 J - V - T under dark conditions

In order to determine the back-contact barrier height, Φ_B , of the microrod devices and to study the junction’s electrical current transport mechanisms, J - V - T measurements in the 250-300 K regime were performed. In Fig. 7.33, $\ln J$ vs V plots of the data are shown

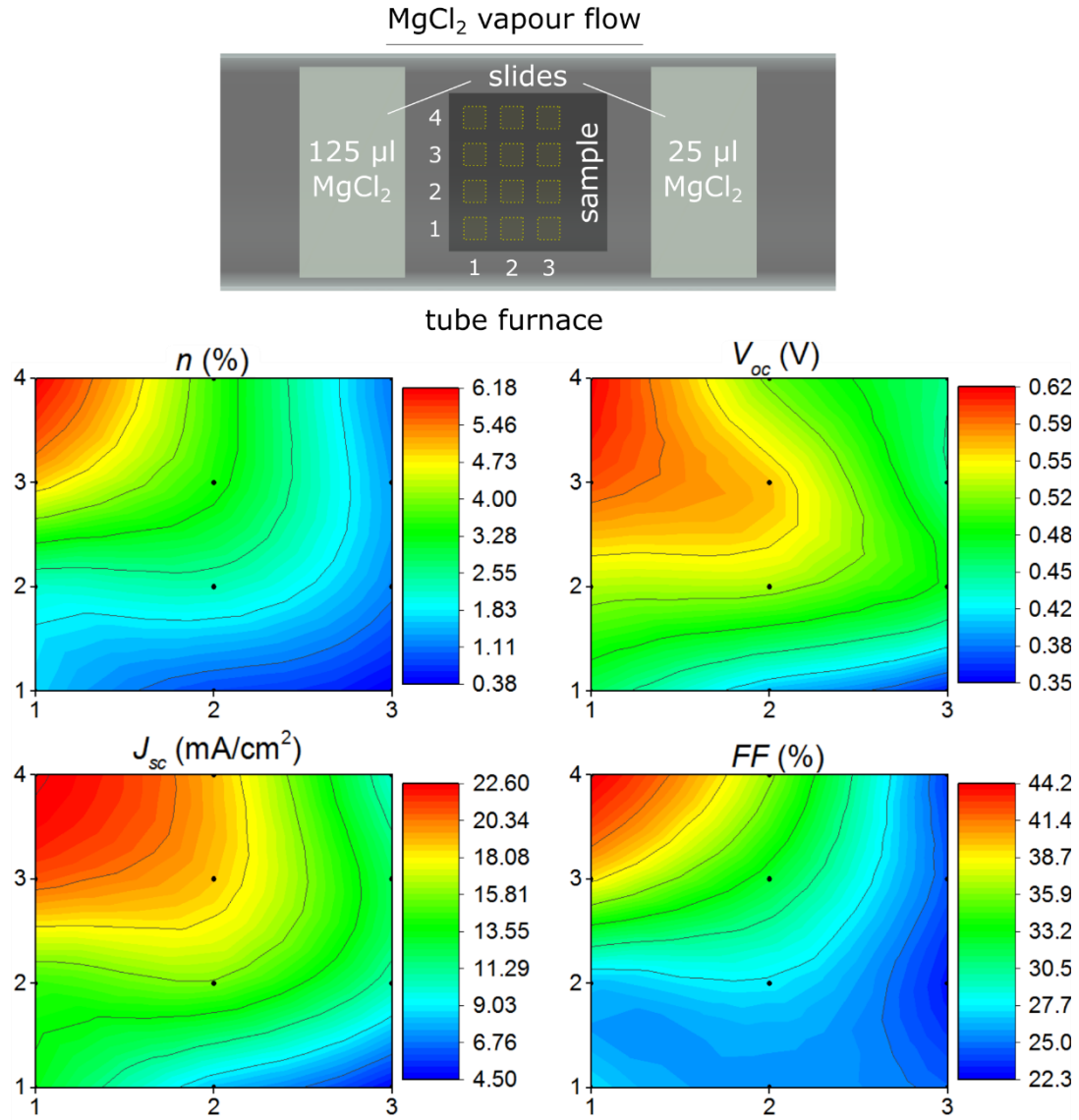


Fig. 7.32 Top: plan view of the sample geometry used for exposing solar cell samples to MgCl₂ vapour in a tube furnace during heat-treatment. Contour maps: J - V curve extracted η , V_{oc} , J_{sc} and FF values of the highest efficiency microrod cell. The x (1 – 3) and y (1 – 4) values are the contacts' coordinates. The curves are smoothed for better visualisation of the performance variations across the total number of contacts

divided in three distinctive regions. Similar to the planar devices J - V - T analysis (Section 7.3.5.2) only data in Region II were amenable to linear fitting.

The extracted n and J_0 values were plotted against temperature and are shown in Fig.7.34a. The temperature dependence of n and J_0 appear to be linear in the whole temperature range. Similar to the planar devices, a change in the slope of the linear fits

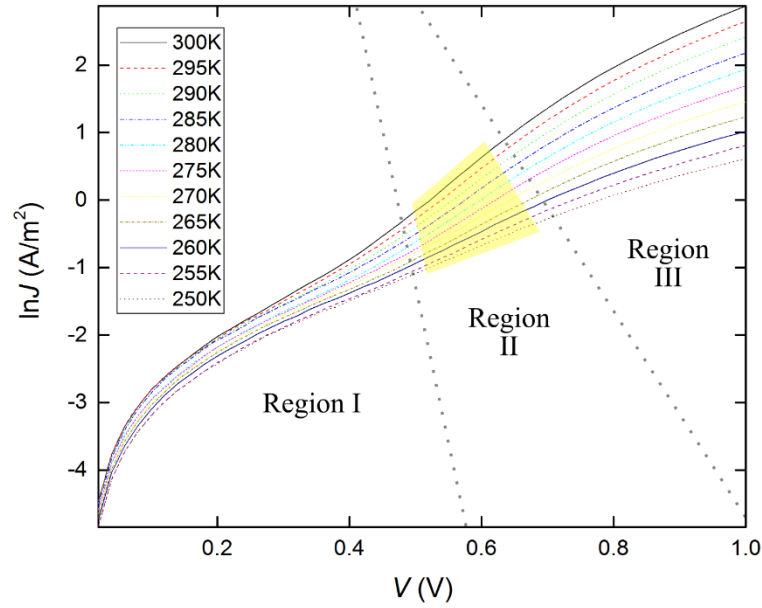


Fig. 7.33 J - V - T analysis of the highest performing microrod CdTe/CdS solar cell: temperature dependent $\ln J$ vs V plot at forward bias demonstrating the low-bias (I), the linear response (II) and the high-bias regions (III)

can be observed around 275 K (5 K higher than the one found for the planar devices).

These findings indicate a multi-step tunnelling mechanism operating in the junction.

The number of tunnelling steps, R , that are required for the tunnelling process can be obtained from Eq. 2.12 (Section 2.2.3.2). For this calculation, the following values were

used: $\epsilon_{\text{CdTe}} = 10.36 \epsilon_0$, $m_n = 0.1 m_e$ ²⁷. C - V measurements of microrod devices were performed and the doping density profile was extracted (Section 7.4.2.4). An average

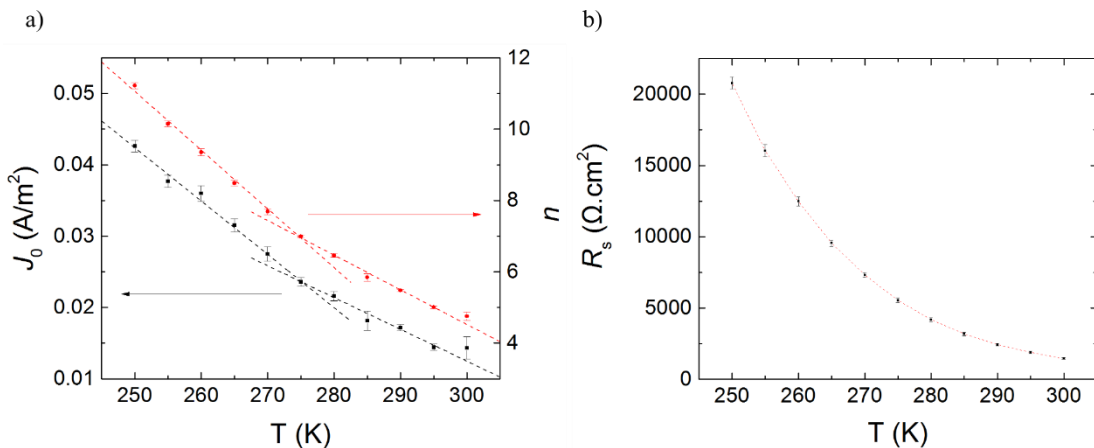


Fig. 7.34 J - V - T extracted a) plot of R_s against temperature used for the back-contact barrier height determination, b) ideality factor, n , and saturation current, J_0 , values plotted against temperature

CdTe doping density of $7 \times 10^{14} \text{ cm}^{-3}$ was estimated from the minimum of the doping density profile plot. Thus, the average number of tunnelling steps at 300 K was calculated to 253 ± 6 . These values are an order of magnitude lower than the steps required for the planar devices.

The method of Bätzner³⁰ was employed (Section 4.4.2) in order to calculate the back contact barrier height of the microrod devices. As shown in Fig.7.34a, temperature dependent R_s values were calculated from the slope of dark J - V curves and plotted against temperature. The barrier height was 0.33 eV by fitting the extracted data to Eq. 4.9. This value is slightly lower than the one calculated for the planar devices (0.41 eV).

7.4.2.3 EQE

Fig. 7.35 shows the response of the highest efficiency microrod device. As for that performed for the planar devices (Section 6.5.2), the spectrum is divided in five spectral regions (I – V) according to the FTO, ZnO, CdS and CdTe absorption edges. Evaluation of the *EQE* response, shows significant losses in regions III and IV. As discussed in Section 6.5.2, losses in these regimes are due to high parasitic photon absorption in the

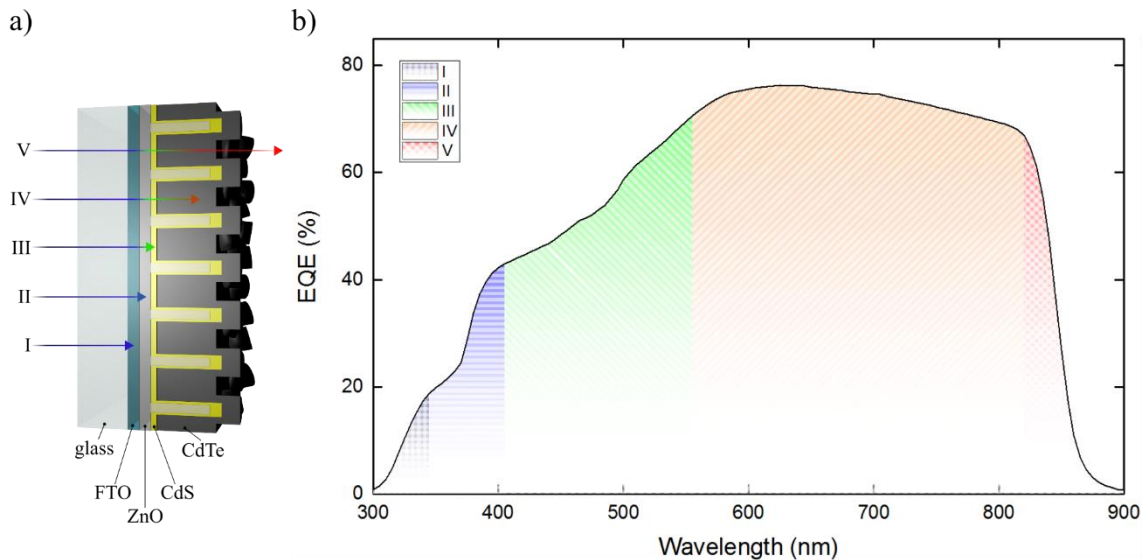


Fig. 7.35 a) Schematic diagram depicting the incident light penetration/ absorption for the five *EQE* spectral regions. b) *EQE* response of the highest efficiency microrod device ($\eta = 6.18\%$). The *EQE* curve is divided in five spectral regions according to the FTO, ZnO, CdS and CdTe absorption edges (boundaries between I – V)

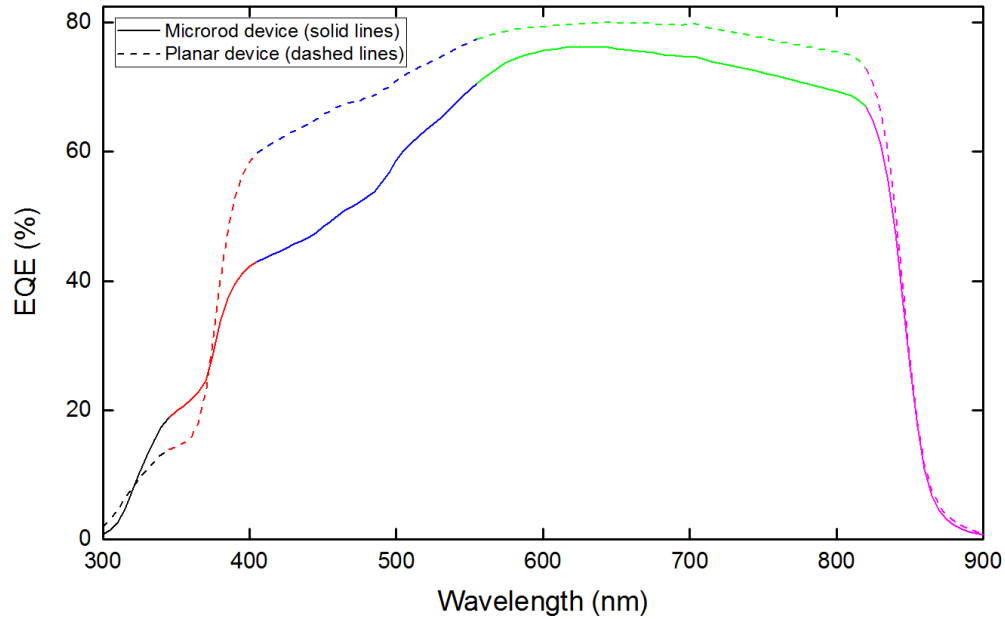


Fig. 7.36 Comparison of microrod (solid lines) and planar (dashed lines) device EQE response. The black, red, blue, green and magenta colours represent the five spectral regions as discussed in the text.

window layer of the device. Indeed, the thickness of the CdS layer of the measured microrod device was 90 nm. The short-circuit current density value was extracted from the *EQE* response and was found to be 23.1 mA/cm^2 , i.e. slightly higher than the *J-V* value of 22.56 mA/cm^2 . The spectral response of planar and microrod devices was compared and is shown in Fig. 7.36. As can be seen, the average *EQE* response of the microrod devices is lower overall. In particular, the planar devices exhibit a lower *EQE* response for wavelengths less than $\sim 370 \text{ nm}$ and a higher response for longer wavelengths when compared to the microrod devices.

7.4.2.4 C-V under dark conditions

The doping density profile of the highest efficiency microrod device was extracted from *C-V* measurements performed under dark conditions. The method in Section 4.4.3 was used and the results are presented in Fig. 7.37. A characteristic U-shape can be observed, which is similar to the one observed in Section 7.3.5.4 and often encountered in CdTe thin film solar cells. The average doping density calculated from the bottom of

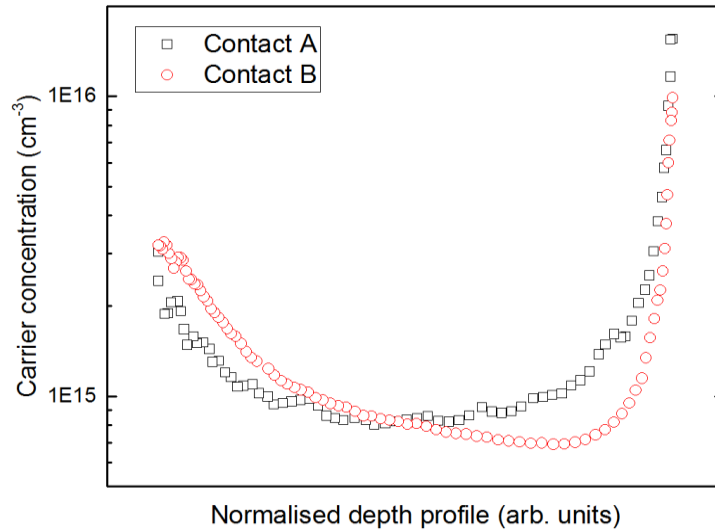


Fig. 7.37 C-V carrier profiles: hole density versus normalised depletion region width plot of two contacts from the highest efficiency microrod CdTe/CdS device ($\eta = 6.18\%$). The normalised depth profile extends from 0 (CdTe/CdS interface) to 1 (near-back surface area)

the U-region was estimated at $7 \times 10^{14} \text{ cm}^{-3}$. This agrees with doping densities of similar devices reported elsewhere^{3,37,38}, but is an order of magnitude higher than the planar devices' doping density found in Section 7.3.5.4.

7.4.2.5 EBIC

Electron beam induced current measurements of FIB cross-sections of microrod devices were performed. In Fig. 7.38a, the frequency-filtered EBIC signal is overlaid on a cross-sectional SEM secondary electron image of the microrod device and shows the location of the PV junction. The frequency filter was applied to minimise noise and fine image detail and the EBIC and SEM image contrast was optimised for a qualitative determination of the junction's position from the location of the EBIC signal. In order to evaluate the average position of the EBIC collection maximum, i.e. the peak of the junction's electric field, a line scan of the frequency-filtered EBIC signal was plotted as a function of beam position relative to the FTO/glass interface (Fig. 7.38b). In the same plot, the average position of the FTO/CdS and CdS/CdTe interfaces which were

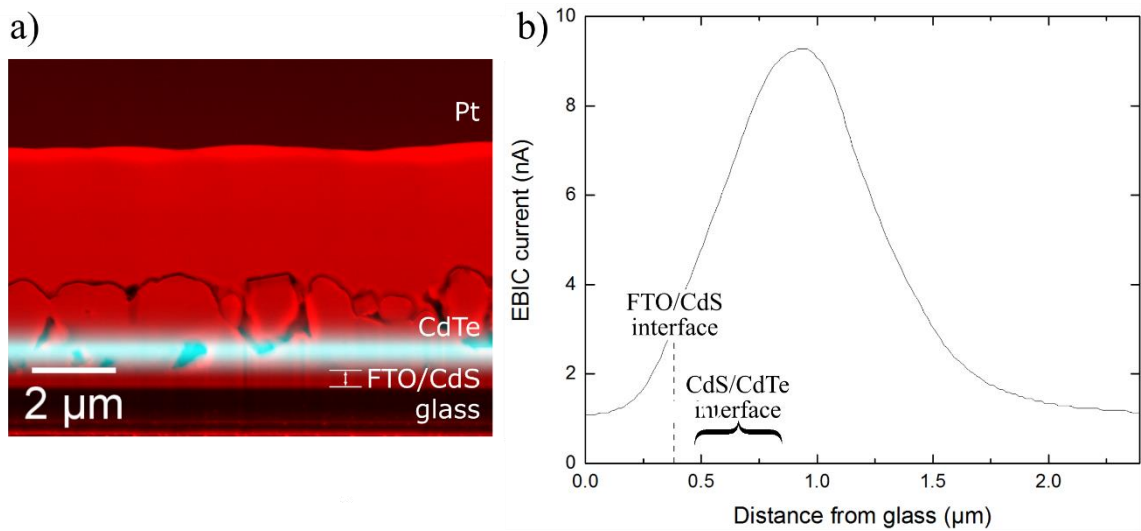


Fig. 7.38 a) Cross-sectional frequency-filtered 8 keV SEM/EBIC secondary electron image overlay of the ZnO microrod CdTe/CdS device. The EBIC signal is coloured in cyan and the secondary electron micrograph in red for enhanced contrast. b) Line-scan plot of the EBIC signal as a function of beam position relative to the FTO/glass interface. The relative positions of the FTO/CdS and CdS/CdTe interfaces were measured from the SEM micrographs using imaging software

measured using open-source imaging software Gwyddion⁸⁷ are shown. The EBIC peak FWHM was 765 nm and the peak centre's distance from the CdS/CdTe interface varied from 50 to 500 nm. Hence the junction is close to the metallurgical CdTe/CdS interface or else is a shallow homojunction.

Fig. 7.39 (right) shows an unfiltered EBIC signal/SEM secondary electron image overlay of the microrod CdTe/CdS device and illustrates the effect of voids and microrods. An inhomogeneous current collection is observed, which appears to be greatly influenced by the topography of the CdS/ZnO microrod layers. Moreover, voids – marked in yellow, blue and green – seem to influence the current collection strongly. Specifically, voids located at discontinuities in the CdS layer (yellow circled area) have an enhanced EBIC signal, while voids in the CdTe absorber layer (blue and green circled areas) correlate with reduced or zero EBIC signal. Moreover, ZnO microrods

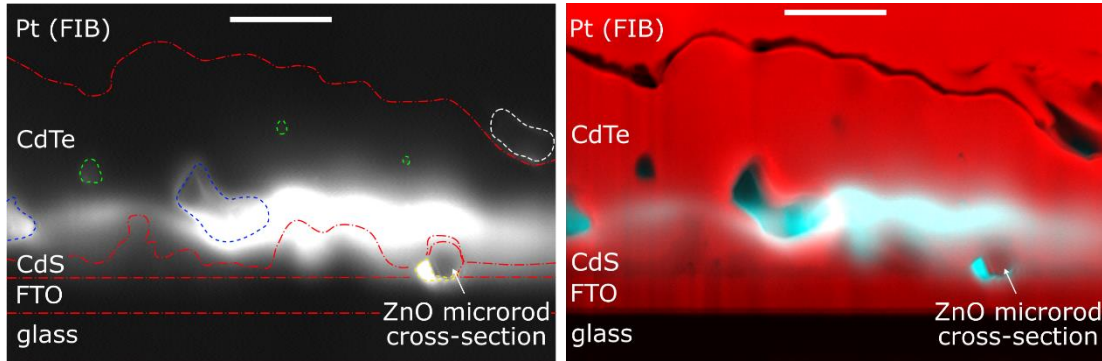


Fig. 7.39 Cross-sectional 8 keV EBIC (left) and SEM/EBIC secondary electron image overlay (right) of the ZnO microrod CdTe/CdS device. The EBIC image contrast and brightness levels were adjusted to visualise minimal current collection and, thus, the PV junction signal is oversaturated. Voids in the CdTe and CdS layers (marked in yellow, blue and green) with different EBIC contrast are observable. current collection is recorded in the white circled area, although it is located outside the CdTe layer. The scale bar length is 1 μm .

had zero contribution to the EBIC signal. This suggests that they act purely as carrier channels with no additional increase in the J_{SC} .

7.4.3 Comparison of planar and microrod CdTe/CdS devices by means of Raman and optical spectroscopy

In this section, Raman and optical spectroscopy comparative analyses of planar and microrod devices are presented. The samples used for these measurements are shown on tables 7.15 and 7.16.

7.4.3.1 Raman spectroscopy

Representative Raman spectra of the measured samples are shown in Fig. 7.40. In Fig. 7.40a, the ZnO microrod and thin film layer spectra are compared and there are peaks at 72, 90, 104, 125, 248, 288, 333, 441, 559, 579 and 637 cm^{-1} (average values). The peaks at 104, 288, 333, 441 and 579 cm^{-1} can be assigned to E_2^{low} , A_1 , $E_2^{high} - E_2^{low}$ (multiphonon), E_2^{high} , E_1/A_1 (LO) respectively^{88–90}. Since the remaining peaks cannot be ascribed to other ZnO vibrations, it is highly probable that their source of origin is the underlying FTO layer or other contaminants. Indeed, the peak 637 cm^{-1} can be

Table 7.15 Samples in the microrod geometry used for the Raman and optical spectroscopy measurements

Sample	ZnO microrods length/diameter (nm)	CdS thickness (nm)	CdTe thickness (nm)
MR1	1000/400	-	-
MR2	1000/400	90	-
MR3	1000/400	90	2000

Table 7.16 Samples in the planar geometry used for the Raman and optical spectroscopy measurements

Sample	ZnO thickness (nm)	CdS thickness (nm)	CdTe thickness (nm)
PL1	80	-	-
PL2	80	45	-
PL3	80	45	1800

correlated to the A_{1g} mode of SnO_2 ⁹¹. Finally, since the peaks at 72 and 90 cm^{-1} are evident in all three plots of Fig. 7.40, they may be ascribed to a systematic measurement error such as contamination. Most importantly, the spectra from planar samples were homogeneous while those from microrod devices showed some spatial variation.

In Fig. 7.40b, the Raman spectra of the CdS coated microrod ('MR2') and planar film ('PL2') samples are presented. The main Raman peaks of CdS appear at 300 cm^{-1} (1LO) and 600 cm^{-1} (2LO)^{92,93}. The peaks at the low end of the spectrum cannot be assigned. Contrary to the ZnO microrods, both planar and microrod CdS coated samples demonstrated very similar Raman spectra since in this case the growth method of the uppermost layers was identical.

For a detailed analysis of the Raman spectra of planar CdTe/CdS devices before and after the MgCl_2 activation step, the reader is referred to sections 7.3.3.1 and 7.3.6.2. In Fig. 7.40c, Raman spectra of complete CdTe/CdS devices adopting the planar and the microrod geometry are presented. Although there are not significant differences between the 'planar' and the 'microrod' spectra, small variations can be observed in the

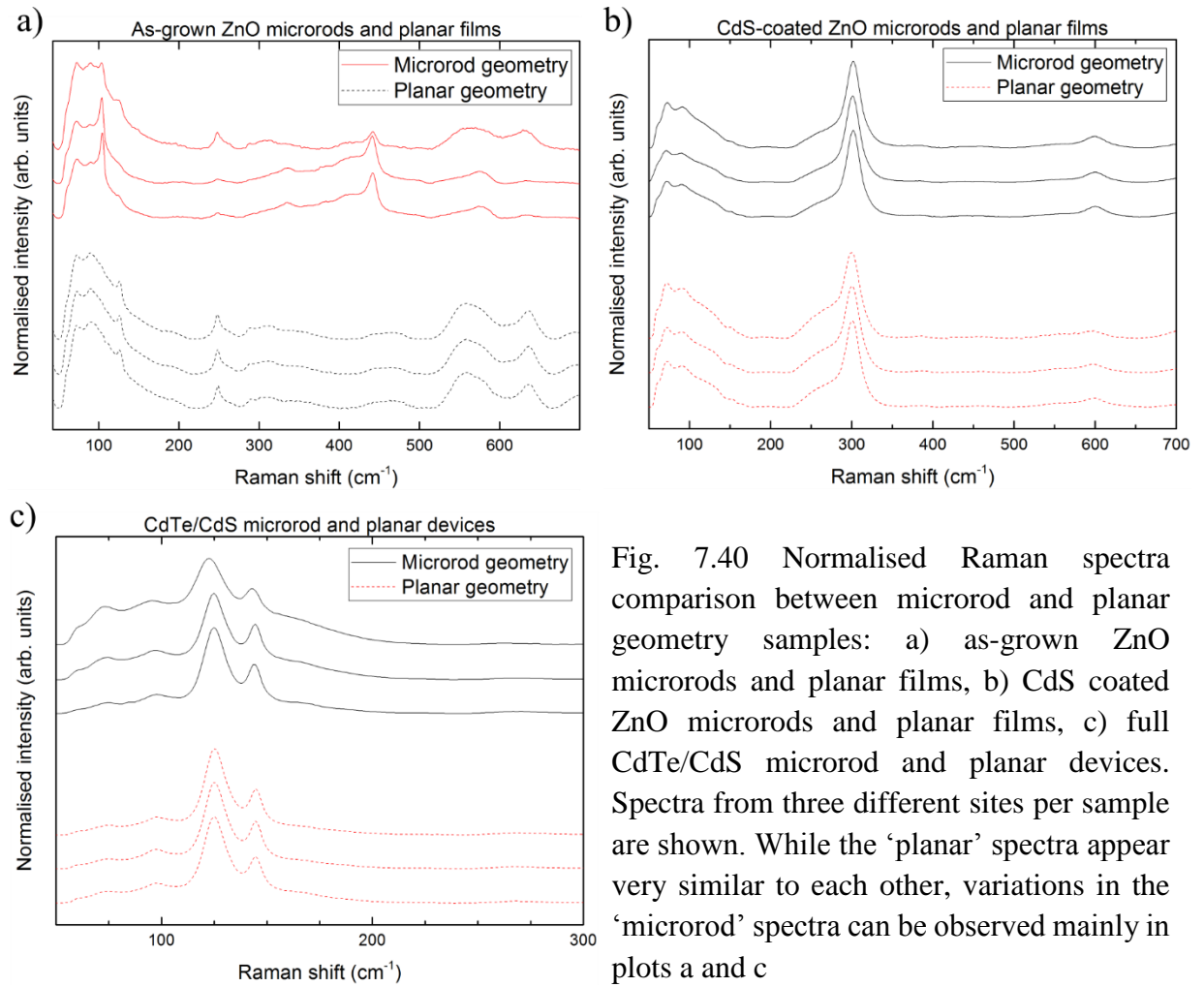


Fig. 7.40 Normalised Raman spectra comparison between microrod and planar geometry samples: a) as-grown ZnO microrods and planar films, b) CdS coated ZnO microrods and planar films, c) full CdTe/CdS microrod and planar devices. Spectra from three different sites per sample are shown. While the ‘planar’ spectra appear very similar to each other, variations in the ‘microrod’ spectra can be observed mainly in plots a and c

peaks’ positions and intensities of the ‘microrod’ spectra. Similar variations were observed in MgCl_2 treated and untreated planar devices.

7.4.3.2 Optical spectroscopy

In order to investigate the optical properties of the microrod geometry and its anti-reflection potential, a series of optical transmittance, specular and diffuse reflectance measurements were performed and are shown in Fig. 7.41. T , R and R_{dif} measurements of as-grown ZnO planar films and ZnO microrods are shown in plots a, c and e, while the spectra of planar and microrod CdTe/CdS full devices are compared in plots b, d and f.

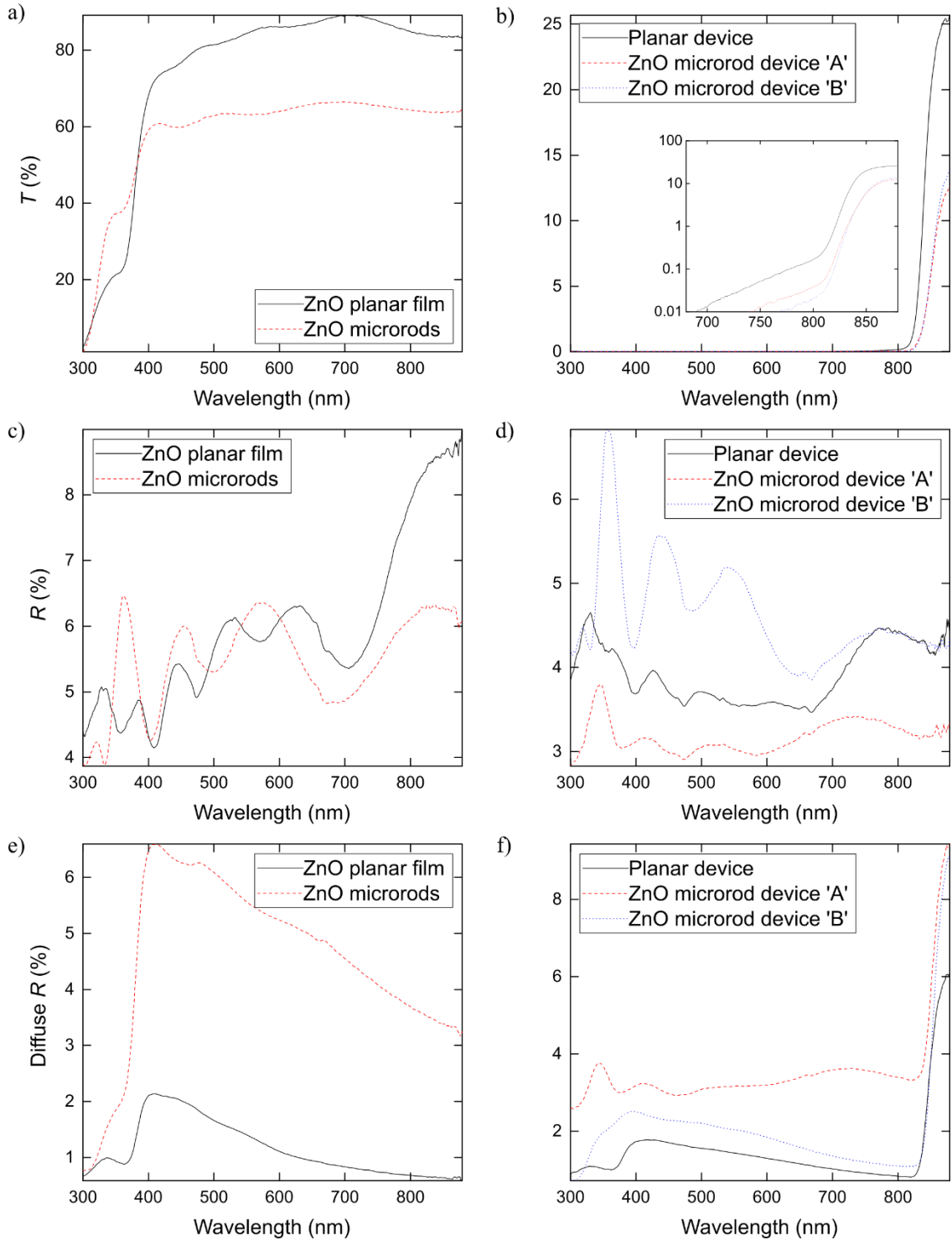


Fig. 7.41 Transmittance (a, b), reflectance (c, d) and diffuse reflectance (e, f) plots of samples adopting the planar and microrod geometries. A comparison of the optical properties of ZnO planar films and ZnO microrods is shown in plots a, c and e, while planar and microrod CdTe/CdS full devices are being compared in plots b, d and f. In plot b, the same transmittance data are plotted using a logarithmic scale in the Y axis in the inset

In Fig. 7.41a, the average transmittance of as-grown ZnO planar films appears to be ~ 15% higher than that of the ZnO microrods. In particular, the ZnO planar films have on average ~ 9% lower transmittance for $\lambda < 385$ nm and ~ 19% higher transmittance for $\lambda > 385$ nm. This may be ascribed to differences in the optical properties of the two TEC substrates used, i.e. Pilkington NSG TEC C15M (planar devices) and Hartford Glass TEC15 (microrod devices) or to scattering losses because of the microrod geometry. Such effects could be detrimental to PV devices that incorporate ZnO microrod arrays by reducing the J_{SC} . Therefore, specular and diffuse reflectance measurements of the same samples were performed and are shown in Fig. 7.41c and Fig. 7.41e. The ZnO microrods and planar films demonstrated similar average specular reflectance values of ~ 6% across the measured spectrum. Moreover, both spectra exhibited a series of interference fringes due to the ZnO/FTO and FTO/glass interfaces. On the contrary, evaluation of the diffuse reflectance measurements (Fig. 7.41e) show a ~ 4% higher average reflectance for the microrod sample. These findings suggest that such ZnO microrod arrays have overall inferior optical properties for PV applications than the equivalent planar films. On the contrary, reports on the use of similar ZnO microrods for CdTe solar cell applications show enhanced optical properties, which led to improved current collection^{94,95}. Tauc plots (Fig. 7.42a,b) were used for the calculation of the ZnO bandgap energy for both the microrod and planar samples. For the planar samples, a strong absorption was found at $\sim 3.2 \pm 0.1$ eV, while for the microrod samples at $\sim 3.1 \pm 0.1$ eV. Both values are in good agreement with the ZnO bandgap values reported elsewhere varying between 3.1 eV to 3.3 eV⁹⁶.

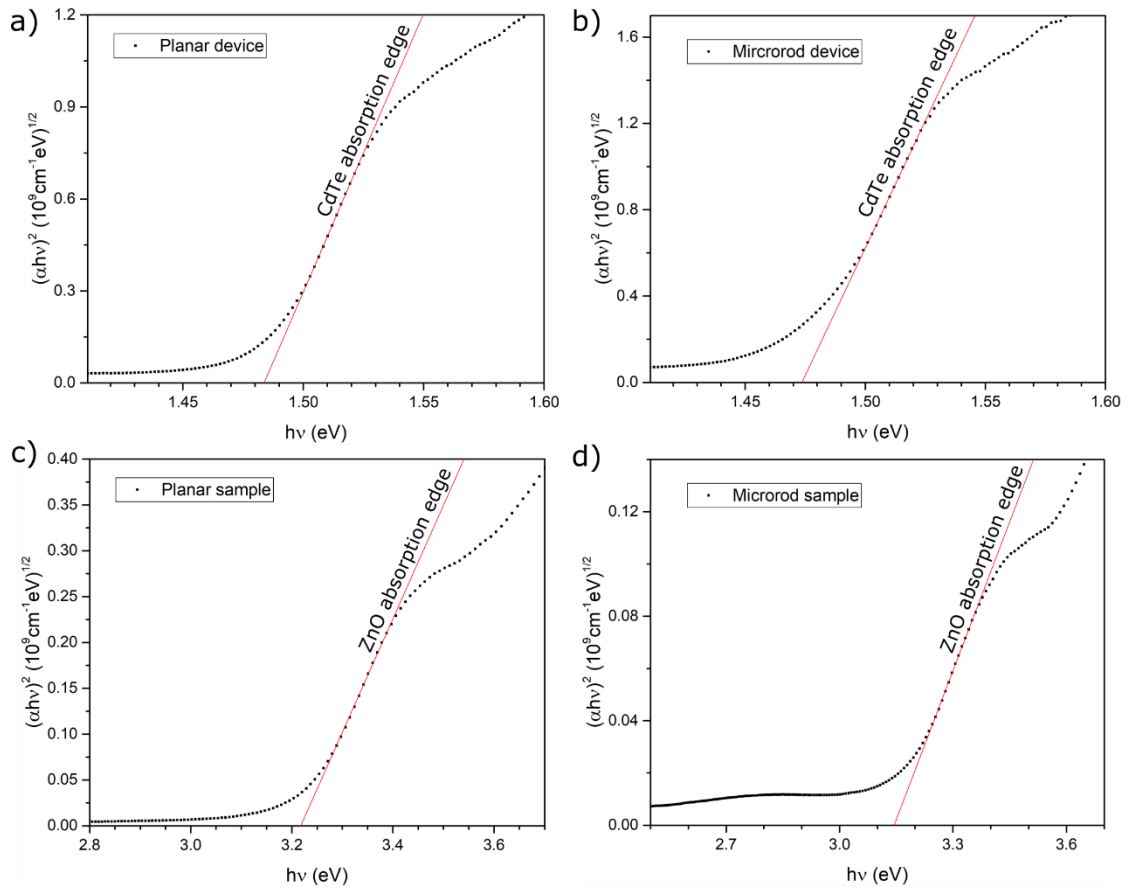


Fig. 7.42 Tauc plots used for the calculation of the ZnO (a,b) and CdTe (c,d) bandgap energies of planar (a,c) and microrod (b,d) samples. The optical band gap is determined from the x -intercept of the linear line fits (red lines).

A similar set of measurements were performed for complete CdTe/CdS solar cell devices. While planar device measurements were consistent for all measured samples, site-to-site and sample-to-sample significant variations were observed in the microrod device measurements. Thus, the plots chosen for presentation show results of only one planar device and two microrod devices ('A' and 'B'). Both microrod devices have the same configuration as sample 'MR3' of Table 7.15. The transmittance plot (Fig. 7.41b) show $< 1\%$ transmittance for all measured devices below 820 nm. The CdTe bandgap was calculated from Tauc plots (Fig. 7.42c,d); for the microrod devices it was $1.47 \pm 0.03 \text{ eV}$ and for the planar devices $1.48 \pm 0.02 \text{ eV}$. These CdTe layers with thickness close to $2 \mu\text{m}$ demonstrated very strong absorption for energies above the CdTe bandgap

as expected. The average specular reflectance was calculated from the plots in Fig. 7.41d and was found to be $\sim 3\%$ for microrod device 'A', $\sim 5\%$ for microrod device 'B' and $\sim 4\%$ for the planar device. In Fig. 7.41f, both microrod devices demonstrated higher average diffuse reflectance of $\sim 4\%$ and $\sim 2\%$, while the average diffuse reflectance of the planar device was $\sim 1\%$. Similar to the findings of the previous paragraph regarding the optical properties of as-grown ZnO microrod arrays and ZnO planar films, the microrod complete CdTe/CdS solar cells demonstrate inferior optical properties for PV applications as compared to the planar control devices. Particularly, such optical losses may be expected to have a significant impact on the J_{SC} values of the microrod devices.

7.4.4 Discussion of microrod materials and devices and comparison with planar devices

ZnO microrod based CdTe/CdS solar cells were fabricated with a peak efficiency of $\eta = 6.18\%$. To the best of our knowledge, this is the highest reported efficiency for solar cells having this configuration. Moreover, a novel feature of this work was the employment of the $MgCl_2$ activation treatment instead of the widely used $CdCl_2$ for the optimisation of the solar cells.

7.4.4.1 ZnO microrod CdTe/CdS solar cell morphology

According to the SEM investigation of Section 7.4.1, a successful conformal coating of the ZnO microrods with CdS and CdTe layers was achieved by means of RF sputtering. However, the cross-sectional SEM micrographs of complete microrod CdTe/CdS solar cells reveal non-uniformities and discontinuities in the CdS layer and the formation of numerous voids throughout the whole of the layer stack.

Non-uniformities in the CdS layer and voids in the CdS/ZnO interface are often encountered in overtreated CdTe/CdS solar cells during the Cl activation process⁹⁹. The CdTe/CdS intermixing that occurs at the MgCl₂ treatment mainly (and in smaller extent at the CdTe deposition) causes the consumption of the CdS layer. However, according to Albin *et al.*¹⁰⁰, a uniform thinning of the CdS layer is expected. However, the samples in this work show significant variations in the CdS thickness and extensive voiding. One factor that leads to a non-uniform CdS layer is the recrystallisation and grain growth that occurs at high temperatures. A second factor that may lead to the formation of voids is the Kirkendall effect¹⁰¹; in the case of asymmetric diffusion fluxes of S and Te atoms Te ($|J_S| > |J_{Te}|$) across the CdTe/CdS interface, the metallurgical interface may move inside the CdS layer leading to the thinning of the CdS. In the extreme case, that such a movement is not possible, voids may be formed. Lastly, an additional contribution comes from shadowing effects during the sputtering process which result in non-uniformities and discontinuities in the CdS layer.

As seen in sections 7.3.3.1 and 7.4.1, untreated sputtered CdTe films exhibit a certain degree of porosity with gaps appearing between the grains. During recrystallisation and grain growth of the CdTe at high temperatures, coalescence of grains and grain boundaries that meet in large angles may lead to the formation of voids in the CdTe film^{58,60,102,103}. Moreover, in the case of the microrod geometry, the ZnO microrods add additional degrees of complexity in the grain structure; pinning of the grains due to the neighbouring microrods and stress-induced effects. Therefore, the development of large voids is expected to be more prominent, resulting in a higher degree of porosity.

7.4.4.2 EBIC investigation of the ZnO microrod CdTe/CdS solar cell

The electron beam induced current investigation of the microrod cells allowed the determination of the PV junction location as well as the impact of the voids in the PV

performance. Evidently, the PV junction formation was found to be strongly influenced by the topography of the CdS/ZnO microrod layers and the voids (Fig. 7.38, Fig. 7.39). Moreover, PV performance measurements showed significant spatial variation on a given device from contact-to-contact. Also, it is not clear if the PV junction is an actual heterojunction or a shallow ‘buried’ homojunction or a combination of them throughout the whole device. Although the *EQE* response for this device did not show any evidence of a ‘buried’ homojunction, the sensitivity of the *EQE* measurements to junction position is limited by the minority carrier diffusion length and may not identify a shallow ‘buried’ junction if present.

All voids apparently demonstrate enhanced EBIC collection, which decreases with increasing void – FTO/CdS interface distance (white, green, blue and yellow circled areas of Fig. 7.39). This signal intensity – distance dependence can be correlated to the carrier diffusion length of CdTe which is typically close to 1 μm . Notably, the white circled area represents a gap between the CdTe layer and the Pt layer used in the FIB milling, which suggests that such a contribution in the EBIC signal is a measurement artefact. An additional contribution to the EBIC signal may come from secondary electrons generated by the interaction of the incident beam with the sample. Secondary electrons generated inside the voids have a higher probability of reabsorption, which may result in higher EBIC collection. Moreover, gaps that lay along the FTO/CdS interface demonstrate enhanced current collection, which may be ascribed to shunting effects due to the discontinuities in the CdS layer. Therefore, we conclude that the origin of the current collection in the voids can be either a measurement artefact or a direct channelling of the incident electrons to the measuring contacts through shunting pathways.

7.4.4.3 Performance losses in the microrod devices

A comparison of the microrod and planar J - V curves under light and dark conditions shows significant losses in all PV parameters. One of the performance limiting factors is the lower $V_{OC} = 0.62$ V of the microrod device as compared to the $V_{OC} = 0.81$ V of the planar device. These reduced V_{OC} values can be ascribed to a high density of shunting pathways due to the large number voids and the discontinuities observed in the CdS layer of the microrod devices. The shunt resistance of the microrod devices was $R_{SH} = 190 \text{ } \Omega \cdot \text{cm}^2$ and that of the planar devices $R_{SH} = 2076 \text{ } \Omega \cdot \text{cm}^2$. Although the back-contact barrier height of the planar devices, $\Phi_B = 0.41$ eV, is higher than that of the microrod devices by 0.8 eV, ‘rollover’ effects which may lead to V_{OC} losses for the planar devices were not observable.

Another dominant performance limiting factor of the microrod device is the poor FF values, which is also influenced by the very low R_{SH} . Additional contribution to the low FF comes from the $R_S = 14.2 \text{ } \Omega \cdot \text{cm}^2$ of the microrod device, which is relatively high compared to the $R_S = 4.33 \text{ } \Omega \cdot \text{cm}^2$ of the planar device. The high R_S values of the microrod device may be attributed to the thicker CdS layer, higher back contact resistance because of the CdTe surface roughness or enhanced intrinsic resistance in the ZnO microrods.

The J - V extracted short-circuit current values were equal to $J_{SC} = 26.1 \text{ mA/cm}^2$ for the planar and $J_{SC} = 22.56 \text{ mA/cm}^2$ for the microrod devices. Fig. 7.36 shows an EQE spectra comparison between the microrod and the planar devices with the average EQE response of the microrod devices being lower overall. In particular, the planar devices exhibit a lower EQE response in the blue regime and a higher response for longer wavelengths when compared to the microrod devices. A similar trend was observed in the comparison of the transmittance of as-grown ZnO microrod and planar samples (Fig.

7.41a). Thus, the lower average *EQE* response of the microrod device can directly correlate to optical losses in the front of the device, i.e. TEC glass/ZnO microrod layer stack. Such losses are either due to parasitic absorption or enhanced reflectance of the incoming photons in the TEC glass/ZnO microrod layer stack. Indeed, the specular and diffuse reflectance measurements show enhanced reflectance both in bare ZnO microrod samples and full microrod devices. The enhanced reflectance may be attributed partly to variations in the optical properties of the two different TEC glass substrates used in the microrod and planar devices. Furthermore, higher internal reflection effects in the glass/FTO and FTO/ZnO interfaces may contribute to the enhanced reflectance as well. Additional *EQE* losses can be observed in the 380 to 550 nm regime because of enhanced photon absorption in the CdS layer. Due to the complexity of the microrod geometry, a thicker CdS layer was required to achieve a sufficient CdS coating of the microrods and to minimise the shunting pathway density. Thinner CdS coatings resulted in significant PV performance losses. Nevertheless, the short-circuit current was not considered to be a major performance limiting factor.

The above findings contradict the *J-V-T* and *C-V* results; the higher CdTe doping density and the smaller number of steps required for the multistep tunnelling in microrod devices as compared to the planar suggest an overall higher material and junction quality. However, the estimation of the correct doping density values from the *C-V* measurements is very crucial, since it is a dominant factor in the calculation of the number of tunnelling steps. That value is therefore subject to any errors in carrier density measurement.

7.4.4.4 Comparison of highest efficiency microrod device to core-shell ZnO/CdTe microrod devices

A thorough search of relevant literature regarding ‘superstrate’ CdTe/CdS solar cells developed on ZnO microrods yielded only four related articles. A comparison to the highest efficiency microrod device reported in this work with $\eta = 6.18\%$, $V_{OC} = 0.62$ V, $J_{SC} = 22.56$ mA/cm², $FF = 44.16\%$ sets it as the record device in this specific configuration. Major *et al.*⁹⁵ devices comprised similar ZnO microrod arrays, RF sputtered CdS layers and CSS deposited CdTe layers with the best device PV parameters being $\eta = 3.49\%$, $V_{OC} = 0.36$ V, $J_{SC} = 21.73$ mA/cm², $FF = 44.63\%$. Similar devices with a different configuration⁹⁴ though reported by Major *et al.*, exhibited efficiencies up to 9.53% and V_{OC} values of 0.76 V, J_{SC} of 19.76 mA/cm² and FF of 65.25%. In Major’s work, the CdS coated ZnO microrods are not embedded inside the CdTe layer, but rather the CSS-deposited CdTe layer ‘sits’ on the tips of microrods. Devices incorporating microrods with lengths from 250 to 2000 nm were investigated demonstrating decreasing PV performance with increasing microrod length. Other reports^{104,105} on ZnO/CdTe/CdS core-shell solar cell devices, i.e. with CdTe nanorods demonstrate very low efficiencies of $\sim 1\%$.

7.5 Conclusions

In this chapter, the development, optimisation and characterisation of planar and microrod all-sputtered ‘superstrate’ CdTe/CdS devices was shown. First, the effect of the CdS and CdTe layer thicknesses on the PV performance of planar devices was demonstrated in sections 7.3.1 and 7.3.2. The optimal CdS thickness was found to be 45 nm. Thinner CdS layers caused shunting between the CdTe and FTO layers, significant deterioration of the junction quality and V_{OC} and FF losses, while thicker CdS layers resulted in optical losses due to parasitical absorption in the CdS for $\lambda < 500$

nm. The effect of the CdTe layers with thicknesses from 0.9 μm to 1.6 μm was evaluated using J - V and EQE measurements. Decreasing CdTe layer thickness resulted in an overall decrease of all PV parameters, η , V_{OC} , J_{SC} and FF . Deterioration of the open circuit voltage and fill factor was ascribed to shunting defects, such as pinholes in the CdTe layer, while the short-circuit current losses were due to photons escaping the device without being absorbed.

In Section 7.3.3, the effects of MgCl_2 treatment and subsequent etching using wet chemical and dry plasma etching techniques were presented. SEM micrographs of as-grown sputtered CdTe films showed a high grain boundary density with gaps across the grain interfaces and poor PV performance ($< 1\%$). On the contrary, evaluation of the MgCl_2 -treated samples by means of SEM and Raman spectroscopy measurements showed a significant reduction of grain boundaries, stress relaxation and the formation of a more compact film due to grain growth and recrystallisation effects. However, post- MgCl_2 SEM/EDX analysis of the back surface revealed the existence of trace amounts of surface impurities, which may account for increased sheet resistance and performance deviations across the samples' contacts. Finally, both N-P and Ar^+ plasma treatments caused severe PV performance deterioration effects due to formation of defects and impurities. On the contrary, pre- and post- Cl activation etching steps were mandatory in order to fabricate high-efficiency CSS-grown CdTe devices (Chapter 6).

Three back contact configurations, Cu/Au, MoO_x/Au and P3HT/Au were investigated as alternatives to Au contacts and the results were presented in Section 7.3.4. While the aim of the Cu, MoO_x layers incorporation was to improve the carrier extraction by lowering the back-contact barrier height, P3HT layers were tested as shunt-blocking layers. The optimal Cu layer thickness was 5 nm and all Cu/Au contacts demonstrated

significantly lower ‘rollover’ effects at high forward bias. On the contrary, the use of MoO_x and P3HT layers always resulted in decline of the PV performance. In particular, the vast majority of the contacts demonstrated distorted *J-V* curves with S-kinks in the first and fourth quadrants caused by interfacial energy barriers and/or reduced carrier mobilities.

The highest efficiency ‘superstrate’-geometry planar CdTe/CdS device demonstrated peak performance parameters of $\eta = 13.28\%$, $V_{OC} = 0.81$ V, $J_{SC} = 26.1$ mA/cm² and $FF = 62.78\%$, which are among the highest reported for all-sputtered devices. The very thin CdS (45 nm) and CdTe (1.8 μ m) layers that were used imply a high-quality deposition process producing smooth, homogeneous films. This resulted in a high spectral response especially for wavelengths above 400 nm with minimal optical losses in the CdS layer. However, devices with so thin CdS may suffer from low V_{OC} values due to high density of pinholes in the CdS/CdTe interface. Thus, further performance improvements could be achieved by substitution of CdS with amorphous CdS:O.

The remaining of this chapter focused on the development and performance evaluation of the microrod devices. ZnO microrods grown on TEC glass with an average density of 10⁴ cm⁻², diameters of 450 nm and lengths of 1 to 2 μ m were successfully coated with CdS and CdTe layers by means of RF sputtering. SEM plan view micrographs revealed both flat areas of CdTe continuous film and CdTe ‘hillocks’ indicating the positions of coated ZnO microrods and planar parts of the sputtered CdTe film. However, the cross-sectional SEM micrographs of MgCl₂-treated complete devices revealed non-uniformities and discontinuities in the CdS layer and extensive voiding throughout the whole of the layer stack. This was ascribed to a combination of shadowing effects during the sputtering process and the complexity of the embedded structure, which

resulted in extensive voiding upon recrystallisation and grain growth during the MgCl_2 treatment.

In Section 7.4.2, ZnO microrod based CdTe/CdS solar cells with $\eta = 6.18\%$, $V_{OC} = 0.62$ V, $J_{SC} = 22.56 \text{ mA/cm}^2$ and $FF = 44.16\%$ were presented, this being the highest reported efficiency for solar cells having this configuration. The main performance limiting factors were the relatively low V_{OC} and FF values, while the PV performance exhibited significant spatial variations on a given device from contact-to-contact. Electron beam induced current investigations showed that the PV junction location was strongly influenced by the topography of the CdS/ZnO microrod layers and the voids. This did not allow to determine with certainty the location of the p - n junction and conclude whether it is an actual heterojunction, a shallow ‘buried’ homojunction or a combination of them throughout the whole device.

To better understand the origin of the performance shortfalls, the PV performance of the best planar and microrod devices were compared. The microrod devices demonstrated very low $R_{SH} = 190 \text{ } \Omega \cdot \text{cm}^2$ compared to the $R_{SH} = 2076 \text{ } \Omega \cdot \text{cm}^2$ of the planar devices as a result of shunting due to the large number of voids and discontinuities. This contributed both to the lower V_{OC} and FF values. An additional contribution to the low FF came from the relatively high $R_s = 14.2 \text{ } \Omega \cdot \text{cm}^2$ of the microrod device compared to $R_s = 4.33 \text{ } \Omega \cdot \text{cm}^2$ of the planar device. This was ascribed to the thicker CdS layer, higher back contact resistance because of the rough CdTe surface and enhanced intrinsic resistance in the ZnO microrods. Finally, EQE and optical spectroscopy measurements demonstrated higher optical losses in the TEC/ZnO/CdS microrod layer stack, which accounted for the lower J_{SC} values. Nevertheless, J_{SC} was not a major performance limiting factor.

Overall, in this chapter all-sputtered planar and ZnO microrod CdTe/CdS devices in the ‘superstrate’-geometry were presented. While the planar devices had efficiencies comparable to those of current record devices, the microrod devices exhibited V_{OC} and FF losses. Nevertheless, this novel device architecture has the potential for further optimisation and significant performance improvements (Chapter 8).

7.6 References

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8 Conclusions and future work

8.1 Research overview, key findings and implications

The goal of this thesis was to explore the potential of NW-based CdTe solar cells to achieve efficiencies similar to or higher than those of planar devices. ZnO microrod based CdTe/CdS solar cells were fabricated with a peak efficiency of $\eta = 6.18\%$ and to the best of our knowledge, this is the highest reported efficiency for solar cells having this configuration. Additionally, there was also incidental new work on application of the recently developed MgCl_2 treatment of ‘substrate’ and all-sputtered ‘superstrate’ CdTe PV devices for the first time.

For the fabrication of nanowires, a broad range of materials and methods were tested for the metal-catalysed and catalyst-free growth of CdTe nanowires (Chapter 5). Although the catalyst-free selective-area growth experiments were less successful, CdTe NW arrays were successfully fabricated using Au and Bi catalysts by means of close-space sublimation (CSS). This is one of the few reports using Au and the first using Bi catalysts for CSS. Extensive trials were conducted using Bi_2Te_3 , Sb, Sn and Pt, but Au and Bi were the most effective. However, Bi was extremely sensitive to

oxidation effects and suffered from reproducibility issues and therefore the preferred route was to use Au.

UV-Vis spectroscopy measurements showed that incorporation of Au-catalysed NWs on CdTe thin-films (200 nm) acted to reduce transmittance from above 10% to below 0.01% and reflectance from above 20% to below 1% (Chapter 6). Similar NW arrays were used for the development of core-shell CdTe/CdS/ITO nanowire solar cells on CdTe-coated Mo foils. Accordingly, planar CdTe/CdS devices in the ‘substrate’ configuration, i.e. Mo/CdTe/CdS/ITO, were developed as a control for the optimisation of the NW solar cells and the evaluation of their performance. High efficiencies were obtained for the planar devices (up to 8.52%), these being very competitive for ‘substrate’ CdTe solar cells. Moreover, this is the first report on the successful use of MgCl_2 instead of the widely used CdCl_2 for the activation treatment of ‘substrate’-geometry CdTe solar cells. A peak efficiency of 2.09% was achieved for the NW devices with MgCl_2 , which is comparable to that of the record device (2.49%) with CdCl_2 . Although further optimisation in terms of NW dimensions, passivation and doping and additional investigations of the nanowire contribution in PV performance are suggested, this is only the second report of NW devices in this specific configuration. Overall, the exceptional optical properties of NWs and their effectiveness to absorb light makes them promising building blocks in the development of very thin devices, where the optical absorption would be otherwise weak.

An alternative solar cell device architecture was demonstrated using ZnO microrods coated with CdS and embedded in a CdTe thin film (Chapter 7). All-sputtered planar ‘superstrate’ devices in the same configuration, i.e. TEC/ZnO/CdS/CdTe/Au, were also fabricated as an optimisation guide and performance control for the microrod devices.

A comprehensive study of the development and optimisation of the planar devices was presented, where MgCl_2 was employed instead of CdCl_2 , this being the first report of its use for the treatment of ‘superstrate’ all-sputtered CdTe solar cells. Planar devices with ultra-thin CdS (45 nm) and CdTe (1.8 μm) layers were presented with efficiencies of up to 13.28%, which are among the highest reported for all-sputtered ‘superstrate’ devices. In addition to this, ZnO microrod based CdTe/CdS solar cells with a peak efficiency of 6.18% were presented, this being the highest reported efficiency for solar cells having this configuration. Using microscopy and spectroscopy analyses, the performance limiting factors for the microrod devices were identified as extensive voiding and, surprisingly, optical losses in the front-most layers of the layer stack. However, this novel device architecture has a great potential for further optimisation and significant performance improvements (Chapter 8). Overall, the results show that MgCl_2 can be used instead of the highly-toxic CdCl_2 for the activation treatment with equally high efficiencies.

8.2 Future work

8.2.1 *Selective-area growth of CdTe nanowires*

- Selective-area growth offers more control than the VLS method over the nanowire dimensions and, importantly, its diameter. In this way, the nanowire dimensions and the optical properties of the nanowire arrays can be tailored accordingly for PV applications. In order to overcome the issues identified in this work, templates with smaller gaps, abrupt sidewalls and oxide-free CdTe substrates would be required. This can be achieved using electron beam, UV and nanoimprint lithography and etching techniques. Furthermore, nanowire growth can be further enhanced using alternative CdTe deposition techniques,

such as electrodeposition. Additionally, patterning could be used to form controlled catalyst arrays for subsequent VLS growth.

8.2.2 Metal-catalysed VLS growth of CdTe nanowires

- In this work, the main limiting factors in the metal-catalysed VLS growth of CdTe nanowires and the use of catalysts alternative to gold were the intrinsic limitations of the CSS reactor: oxygen impurities, the low vacuum chamber and lack of independent control of the source and substrate temperature. Alternatively, high or ultra-high vacuum techniques, such as sputtering, MBE and MOVPE could be tested, which may enable a very precise control of the growth rate and the composition.
- As an alternative to the formation of catalyst droplets by dewetting of thin metal films it would also be possible to instead directly spin or drop-cast colloidal suspensions of catalysts particles on the substrate. This may enable a better control over the geometry of the catalyst array and a understanding of the nanowire growth mechanism.
- Photoluminescence, cathodoluminescence and HRTEM/EDX measurements can be used to study the nanowire crystal structure and optoelectronic properties.

8.2.3 ‘Substrate’-geometry nanowire CdTe/CdS solar cells

- One of the remaining questions regarding the performance of the NW CdTe/CdS devices is whether the nanowires or the underlying buffer layer is the main contributor to the photocurrent generation. This requires further investigation and could be achieved using *EBIC* measurements.

- The extent and impact of impurities on the PV performance of NW-based CdTe devices could be evaluated by employing nanowires grown using alternative catalysts to Au or catalyst-free grown nanowires (sections 8.2.1 and 8.2.2).
- As explained in 8.2.1, templated growth potentially offers superior control over the geometry of either the nanowires or the catalyst droplets: this should be exploited in devices fabricated using such materials.
- Techniques that offer a better control over the deposition of the nanowire shell layers should be investigated. For example, CdS and ITO layers with a homogeneous thickness and lower degree of shadowing effects can be achieved by using atomic layer deposition. This may act to reduce electrical shunting.
- Surface states and dangling bonds are extremely important for nanowires with very high surface-to-volume ratio. Thus, surface passivation using thin oxide or semiconductor layers should be investigated.

8.2.4 ‘Substrate’-geometry nanowire and planar CdTe/CdS solar cells

- One of the performance culprits in both nanowire and planar ‘substrate’ devices was the rectifying back contact. Thus, the use of buffer layers or the heavy doping of the CdTe back surface should be investigated.
- For ‘substrate’-geometry solar cells it has been demonstrated elsewhere that inclusion of a ZnO high resistance transparent layer between the CdS and ITO layers yields higher V_{OC} values. This should be explored for the present samples.
- J_{SC} losses can be partly reduced by substituting the CdS with an amorphous CdS:O layer.
- Although the ‘second’ annealing step after the ITO deposition was crucial in achieving high PV performance it may have detrimental effects on the ITO

properties. Thus, its effectiveness at lower temperatures or its implementation at an earlier development stage, i.e. before the ITO deposition should be further investigated.

8.2.5 '*Superstrate*'-geometry microrod CdTe/CdS solar cells

- The main performance inhibitor of the microrod devices was the extensive voiding throughout the whole of the layer stack. This is presumably related to the CdTe deposition, the complexity of the embedded structure and recrystallisation and grain growth phenomena that occur during the MgCl_2 treatment. Therefore, the CdTe growth conditions or alternative deposition techniques which can result in less porous CdTe films, the effect of the microrod array geometrical characteristics and the MgCl_2 treatment conditions should be further investigated. Alternatively, post-growth passivation or void filling approaches could also offer significant performance improvements.
- Optical losses in the front-most layers (TCO and CdS) of the layer stack were observed for the microrod devices. The influence of the TEC glass and the geometry of the microrods on the optical properties of the devices should be investigated.
- A different device architecture can be investigated by using techniques which enable precise thickness control for the deposition of the CdS and CdTe layers, such as ALD. In this way, core-shell ZnO/CdS/CdTe devices can be developed.

8.2.6 '*Superstrate*'-geometry microrod and planar CdTe/CdS solar cells

Both microrod and planar devices can benefit by substituting the CdS with an amorphous CdS:O layer. Due to its wide bandgap, lower optical losses are expected, which can contribute to higher J_{SC} values. Additionally, this enables the use of a thicker

window layer with minimal J_{SC} losses, which can result in V_{OC} improvements due to reduced shunting. In addition to this, a lower degree of interface discontinuities is expected, since a reduced S and Te inter-diffusion has been reported in CdS:O/CdTe layer.

Appendix A: Growth of Bi-catalysed CdO nanowires

A.1. Introduction

Here, a study on the spontaneous growth of VLS Bi-catalysed CdO nanowires is reported. Results on the morphology and elemental composition of the Bi-catalysed CdO nanowires are presented and the growth mechanism of the nanowires is investigated.

A.2. Experimental

Pilkington Optiwhite glass substrates (4 mm thick) were cut to 50 mm × 50 mm, ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N₂ gun. To remove all surface contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and dried with a N₂ gun again. Next, bismuth thin films (1-10 nm) were thermally evaporated on the glass substrates at room temperature with a base pressure of $\sim 10^{-5}$ mbar and a growth rate of $< 1 \text{ \AA/s}$ with the sample stage rotation on. The samples were loaded in the CSS chamber for the nanowire growth. The Bi catalyst dewetting and the NW growth processes were carried out at 460 – 570°C source

temperature, 400 – 560°C substrate temperature, 5 – 40 Torr dynamic H₂ pressure, 0 – 90 minutes. As in the Bi-catalysed VLS growth of CdTe nanowires in H₂ atmosphere (Section 5.5.3), while the use of H₂ was essential in impeding the oxidation of the Bi catalysts, its use caused instability in the CSS CdTe source and irreproducibility issues. The morphology and elemental composition of the CdO nanowires were evaluated using SEM/EDX (the reader is referred to Chapter 4 for more background information on the growth and characterisation methods).

A.3. Results

CdO nanowire growth occurred spontaneously using the same growth conditions as in Section 5.5.3, but with the substrate heater on. In Fig. A.1, a dense array of CdO nanowires grown at $T_{\text{src}} = 470^\circ\text{C}$, $T_{\text{sub}} = 420^\circ\text{C}$, 7 Torr, 50 sccm H₂, 20 mins is shown. The diameters and lengths of ~ 60 nanowires were measured and the average values were 30 ± 9 nm and > 3 μm respectively, while no catalysts could be observed at the nanowire tips. As shown in Fig A.2 (left), CdO nanowires could be detected only in the

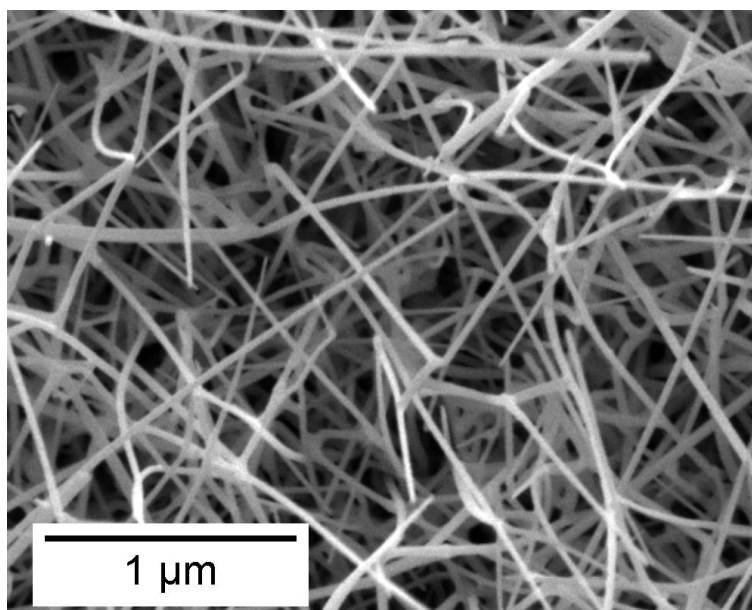


Fig. A.1 Secondary electrons SEM image of Bi-catalysed CdO nanowires. The area under investigation was located < 1 mm away from the sample's edge.

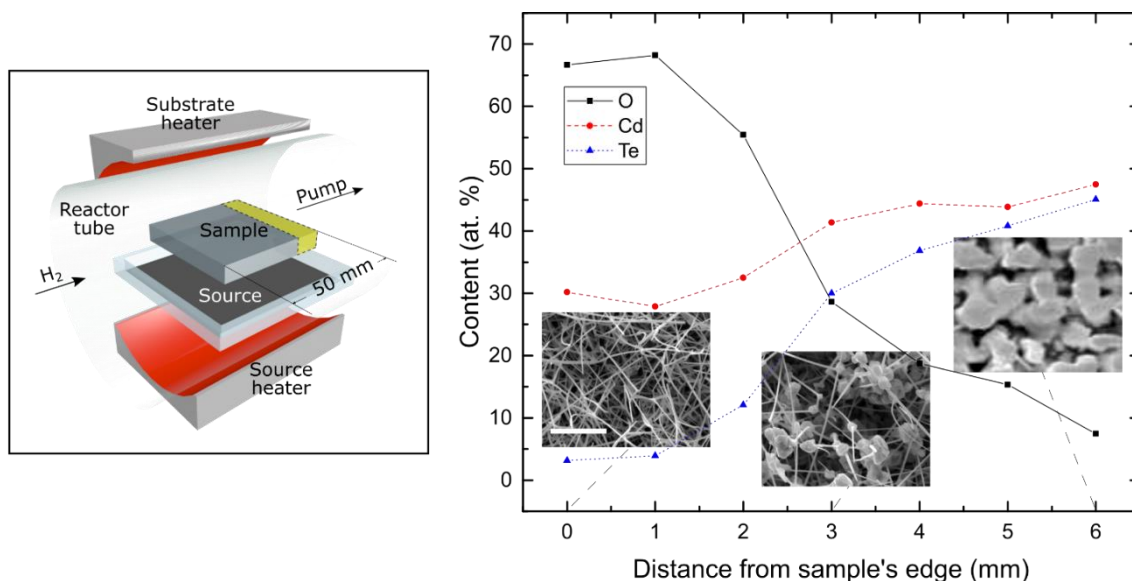


Fig.A.2 Left: schematic of the CSS reactor. CdO nanowires were detected only in the bottom side (facing the CdTe source) of the marked area close to the right edge of the sample. Right: plot of O, Cd and Te at.% at 0 – 6 mm from the sample's edge. Insets: SEM micrographs of the surface morphology. At a distance of > 6 mm from the sample's edge no CdO nanowires could be detected.

marked area (yellow) close to the right edge of the sample. Specifically, the density of nanowires decreased with increasing distance from the sample's edge. At distances greater than ~ 6 mm from the sample's edge, no CdO were detected, but, instead, a rough CdTe thin film was observed.

The surface elemental composition at a distance of 0 – 6 mm from the sample's edge was determined by SEM/EDX area measurements (~ 120 μm^2). The O, Cd and Te atomic content was plotted against varying distance from the sample's edge and is shown in Fig A.2 (right). As can be seen, while close to the edge the sample appears O- and Cd-rich, at distances greater than 6 mm, the oxygen content drops below 10 at.% and an almost stoichiometric CdTe can be observed. According to this and the observation that the nanowire density decreases with increasing distance, it is speculated that the nanowires are made of CdO. This was confirmed by SEM/EDX point measurements at three different points of an individual nanowire (Fig. A.3)

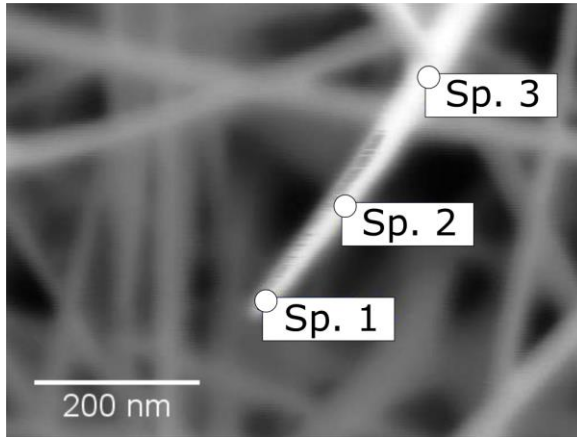


Table A.1 SEM/EDX point measurements at three different sites of an individual CdO nanowire

Spectrum	O (at.%)	Cd (at.%)	Te (at.%)
Sp. 1	43	55	2
Sp. 2	46	49	5
Sp. 3	43	57	0

Fig. A.3 High magnification SEM micrograph depicting the sites used in the EDX compositional analysis of an individual CdO nanowire

According to Table A.1, high atomic concentrations of Cd and O were detected, while the Te content was below 5 at.%. A discrepancy in the measured atomic content of oxygen between point measurements along the nanowires and area measurements of the sample's surface close to the edge was observed. This was ascribed to a higher signal contribution from the substrate in the latter measurements. Indeed, the at.% of Na, Mg, Si and Ca substrate impurities (not shown here) scaled with increasing distance.

A.4. Discussion

The elemental composition of the CdO nanowires was verified using point and area SEM/EDX measurements and a near stoichiometric atomic content of Cd and O was detected. However, in order to explain the growth of CdO nanowires, the reasons for the limited NW growth area, the origin of the oxygen atoms, and the potential growth mechanism were explored. First, the reasons why CdO nanowires were only detected in a very narrow regime of the samples' right edge (Fig A.2), while a standard CSS-grown CdTe film was detected in the rest of the sample's area is discussed. Although edge effects, such as different desorption rates of Cd and Te atoms from the sample's surface could result in variations in the CdTe deposition, a symmetrical growth of CdO

nanowires in all four sample edges would be expected. Moreover, thickness fluctuations in CSS-deposited CdTe thin films often exist because of the variations in the sublimation rate of granular inhomogeneous CdTe sources. However, this factor was ruled out since the CdTe powder source in this work was placed centrally in the source tray and, thus, any thickness fluctuations in the deposited CdTe would be symmetrical. Finally, the initial growth of CdO nanowires throughout the whole sample and the subsequent partial burial with a CdTe thin film was also ruled out, because trace amounts of nanowires would be expected in the other three sample edges. Therefore, it is speculated that the growth of CdO nanowires only close to the sample's edge is related to the gas flow dynamics inside the CSS reactor, the effect of H₂ on the CdTe sublimation and on the transport of Cd, Te and H₂Te atoms, the existence of a possible temperature gradient across the sample in the direction of the gas flow or to the limited supply of oxygen atoms.

The potential sources of the oxygen atoms are now discussed. Since CdO nanowires were grown only on glass substrates, oxygen atoms from the glass could diffuse and combine with Cd adatoms and result in the growth of nanowires. However, this cannot explain the growth of straight CdO nanowires with lengths of tens of micrometres that were observed in this work due to the limited diffusion length of the oxygen atoms. Therefore, it is speculated that a continuous supply of oxygen atoms in the vapour phase is required in order to explain the growth of nanowires of such lengths. Although a high-purity hydrogen flow was used, oxygen impurities in the CSS chamber are expected due to the CSS being a low – medium vacuum process, possible chamber leaks, oxides that exist in the CdTe source or trace amounts of oxygen in the gas lines.

The main studies on the growth of similar CdO nanowires using chemical or physical vapour techniques are now discussed in order to understand the growth mechanism of the nanowires in this work. The growth of CdO nanowires using an Au-catalysed VLS method has been reported by Kuo¹ and Liu². In both cases, it was postulated that in the early stages of the growth process, a supersaturated Au – Cd liquid alloy was formed at a high cadmium atomic percentage. While Kuo¹ suggests that oxygen may diffuse into the droplet, bind with the Cd atoms and precipitate as CdO, Liu² proposes that only Cd atoms diffuse into the droplet, precipitate and, subsequently, react with the O adatoms forming CdO layers. Moreover, Liu suggests that CdO nanowire growth proceeds even with trace amounts of oxygen (0.02% O₂), which maybe the case in this work. Peng³ has reported the synthesis of CdO nanowires with similar lengths and diameters using a Te-catalysed VLS growth method in an oxidising atmosphere. Lastly, the non-catalysed vapour-solid growth of CdO nanobelts has been reported by Pan⁴ using a thermal evaporation process of CdO powders. In all growth studies of CdO nanowires using the catalysed VLS mode, an oxidising atmosphere was used and Au or Te catalysts were detected at the tips of the nanowires. Although catalysts at the nanowires tips were not detected in this work, CdTe deposition was carried out on Bi-coated glass substrates. Therefore, a growth scenario where the CdO nanowires were formed via a Bi- or Te-catalysed VLS growth mode and the catalysts vanished after or during the nanowire growth cannot be ruled out. Indeed, catalyst instability and gradual volume reduction can occur through diffusion, incorporation, evaporation or reaction processes^{5,6}. This is further amplified by the high volatility of bismuth and the formation of hydrides. Moreover, in the findings of Kuo¹, the catalysts had diameters of less than 20 nm. If similarly sized catalysts exist in this work, it is highly probable that the resolution of the employed SEM microscope was not enough to resolve them. Overall,

the growth mechanism of the CdO nanowires in this work cannot be inferred with certainty and further investigations are required.

A.5. Conclusions

CdO nanowire arrays of very high density and aspect ratios were grown on glass substrates in H₂ atmosphere. It was speculated that the growth was influenced by the gas flow dynamics, the effect of H₂ on the CdTe sublimation, the substrate temperature and oxygen impurities, but the growth mechanism could not be inferred with certainty and further investigations are required.

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Appendix B: Assessment of alternative catalysts for the VLS growth of CdTe nanowires

B.1. Introduction

In this section, an overview of the extensive attempts to find alternatives to Au and Bi catalysts is given. A group of materials, namely Bi₂Te₃, Sb, Sn, and Pt was selected and explored, but NW growth was not observed.

B.2. Experimental

Pilkington Optiwhite glass substrates (4 mm thick) and Si wafers were cut to 25 mm × 25 mm, ultrasonically cleaned for 30 mins in de-ionised (DI) water with detergent and dried with a N₂ gun. To remove all surface contamination, the substrates were brushed in DI water, isopropyl alcohol (IPA) and dried with a N₂ gun again. Next, Bi₂Te₃, Sb, Sn, and Pt thin films (2-50 nm) were thermally evaporated on at room temperature with a base pressure of $\sim 10^{-5}$ mbar and a growth rate of $< 1 \text{ \AA/s}$ with the sample stage rotation on. Studies of the formation of catalyst droplets were carried out by annealing catalyst thin films deposited on Si wafers and glass substrates inside the CSS chamber. The

conditions for the CSS chamber annealing experiments were 250-650°C, 5 – 300 Torr of static or dynamic H₂/N₂ ambient for 0-60 minutes. Both substrate and source heaters were used to achieve a uniform heat distribution. The development of catalyst nanodot arrays was investigated using SEM.

B.3. Results

Bi₂Te₃: In order to stabilise the Bi catalysts during CdTe deposition, thin Bi₂Te₃ films were deposited by thermal evaporation and annealed under controlled conditions. However, the deposition of stoichiometric thin films was unsuccessful and thermal annealing resulted in irregular shaped and needle-like features. The problematic generation of Bi₂Te₃ nanodots was ascribed to a combination of lack of control over the film's stoichiometry and oxidation phenomena, which have a strong effect on the surface dynamics and film dewetting during thermal annealing. The use of Bi₂Te₃ for the VLS growth of CdTe nanowires resulted in the spontaneous formation of nanostripes of low densities with irreproducibility issues and lack of control over the growth of the nanostructures.

Sb and Sn: Although Sb and Sn nanodot arrays were successfully generated on glass substrates and Si wafers, CdTe growth resulted in the deposition of a two-dimensional CdTe film without the growth of nanowires. Moreover, Sb and Sn could not be detected after the CdTe deposition. Similarly to the Bi catalyst investigations, this was ascribed to a combination of the following: high volatility of the catalysts, formation of hydrides in the case of H₂ atmosphere, oxidation phenomena in H₂ absence.

Pt: Generation of Pt nanodots was unsuccessful.

B.4. Conclusions

A broad range of materials, such as Bi_2Te_3 , Sb, Sn, and Pt were tested for their suitability in the VLS growth of CdTe nanowires. The development of nanodot arrays and in turn the growth of nanowires was unsuccessful. To this end, further investigations are required using a growth setup, such as an MBE chamber, that could enable the deposition of catalyst thin-films and *in situ* development of nanodot arrays and nanowire growth without braking the vacuum. In this way, the minimisation of oxidation effects can be achieved.

